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Comparison between FLL and PLL in frequency estimation to supply distributed virtual inertia

Erland Novoa[1], Julio C. Tafur[2] and Damian Sal y Rosas[3]

[1] Department of Engineering-
Mechatronic Engineering Master Degree Program
Pontificia Universidad Católica del Perú

[2] Department of Engineering-
Control and Automation Engineering Master Degree Program
Pontificia Universidad Católica del Perú

[3] LAAS-CNRS, University of Toulouse, 31031 Toulouse, France

Abstract. To connect renewable energy sources (e.g. solar or wind) on the grid, an inverter or electronic converter is used. However, a traditional inverter has no inertia in the face of frequency changes. Unlike the inertia of the rotor of a synchronous generator. Frequency variations are a product of the imbalance between the energy generated and the grid loads. If the frequency is too far from its nominal value or if the rate of change of frequency (RoCoF) is high, it can affect the synchronism of the generators that feed the grid. Therefore, power cuts are made in sectors on the grid, thus preventing instability from spreading to other sectors on the grid, which translates into large economic losses. Solutions such as inverters with virtual inertia (or emulated inertia) are a good alternative due to their structural simplicity and low cost, compared to other solutions such as synchronous condensers, for example. For the virtual inertial control strategy, the grid frequency needs to be measured. This article compares the use of a phase-locked loop (PLL) or a frequency-locked loop (FLL) for frequency estimation and its effect on inertia emulation. The proposed control designs are validated through simulations.

Key words. Frequency-locked loop (FLL), Phase-locked loop (PLL), Rate of change of frequency (RoCoF), virtual inertia.

1. Introduction

According to the standards of each country, the electrical grid must maintain a nominal frequency, which must be synchronized with the rotation speed of the synchronous generators (SG) that feed the grid. In the case of Peru, the nominal frequency is 60 Hz with a maximum deviation of 0.36 Hz [1]. Grid quality is measured in the stability of the grid frequency (f). A large SG supports the stability of the grid, since the inertia of its rotor opposes frequency changes [2]. Studies such as [3] emulate the inertia of an SG in the control strategy of an investor, to improve the quality of the grid.

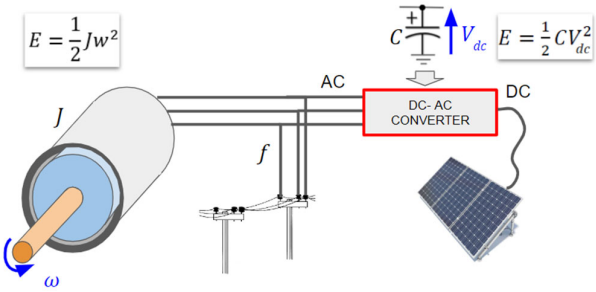

Fig. 1. Comparison between the kinetic energy in a generator with the energy stored in the DC-Link capacitance.

Fig. 1 shows a simplified graphic of a grid-connected SG as well as a grid-connected photovoltaic (PV) panel using a DC-AC converter. It is observed that the rotational inertia of the generator (J) is related to the DC-Link capacitance (C) and the angular speed of the generator (w) is related to the DC-Link voltage (V_{dc}). If f decreases, the SG opposes such a change, since it delivers part of its kinetic energy to the grid, decreasing its w. On the other hand, the PV that uses a traditional DC-AC converter does not detect the change of f and therefore does not oppose such a change. This is a problem since the increase in these energy sources decreases the stability of the grid (or grid inertia). The concept of virtual inertia is based on taking advantage of the energy stored in the DC-Link capacitance (C) to oppose changes of f, like an SG, but in this case discharging its V_{dc}.

What remains of this paper is the control strategy of a traditional grid-connected inverter in section 2. Virtual inertia is then added to the inverter in section 3. In section 4 the frequency estimation between the FLL and the PLL, as well as how such estimation influences inertia emulation. Finally, section 5 concludes the main contributions of this paper.

2. Grid connected inverter

Connecting a photovoltaic panel (PV) to the grid requires a DC-DC converter, a DC bus and an inverter. The inverter has IGBTs that are triggered with 6 PWM signals generated by a controller device. This paper deals with the control strategy of the grid-connected inverter, which is shown in Fig. 2, but it does not deal with the design of the DC-DC converter or the PV.

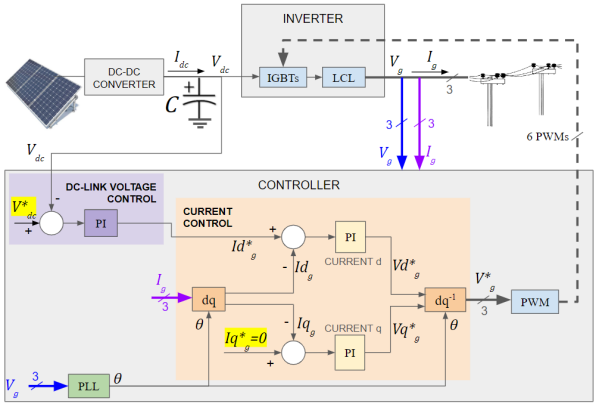

Fig. 2. Inverter that connects a photovoltaic panel to the grid.

If the power of the photovoltaic panels is increased, the DC-Link voltage (V_{dc}) tends to increase. However, if more three-phase current is injected into the grid (I_g) by discharging the DC-Link capacitors, V_{dc} would be regulated. On the other hand, in a power decrease situation, V_{dc} tends to decrease. In this case, I_g must be decreased to regulate V_{dc}. Therefore, to connect an inverter to the grid it is necessary to control the DC-Link voltage at a desired value (V_{dc}^*) in cascade with the control of I_g. n this paper, the superscript * is used to indicate the desired value in a control loop. Regarding the control of I_g, the dq and dq^{-1} transforms are used, which require the grid phase (θ) as an input parameter. The estimate of θ is obtained from sensing the three-phase grid voltage (V_g), using a PLL.

A. PLL design

Fig. 3 shows the internal structure of the PLL of Fig. 2, noting the use of the dq transform followed by proportional integral (PI) control.

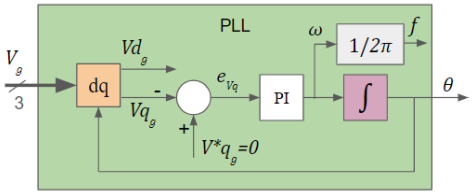

Fig. 3. PLL block.

If the q component of the grid voltage (Vq_g) is zero, the phase of the grid (θ_g) would be equal to the rotation angle (θ) of the coordinate system dq. Such a statement is verified graphically in Fig. 4 and explains the control loop of Fig. 3, also known as synchronism control.

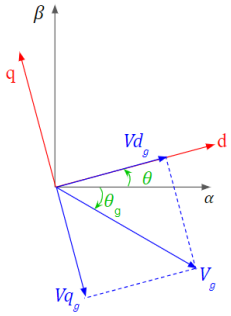

Fig. 4. Vector representation of the dq transform of V_g.

After linearizing when $\theta \to \theta_g$, the PLL loop in Fig. 3 is transformed into the loop in Fig. 5. In which the dynamics of the digital processing delay time (T_r) and the parameters of the PI control (K y T_i).

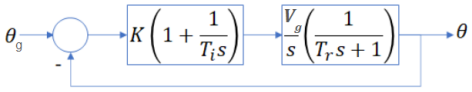

Fig. 5. Modified PLL.

The open-loop transfer function of Fig. 5 is expressed in (1).

$$L(s) = \frac{KV_g}{T_i s^2}\left(\frac{T_i s + 1}{T_r s + 1}\right) \tag{1}$$

The PI control parameters are determined using (2) and (3) and are obtained after applying the Symmetric Optimum Method, in which the symmetry of the Bode plot of $L(s)$ and the maximum phase are used for the cutoff frequency (ω_c).

$$T_i = \frac{1}{\omega_c^2 T_r} \tag{2}$$

$$K = \frac{\omega_c}{V_g} \tag{3}$$

Table I, shows the system variables and the obtaining of the PI control parameters when applying (2) and (3).

Table I. PLL control design parameters.

System variables	PI control parameters
$V_g = 179.6\,V$ $\omega_c = 1131\,rad/s$ $T_r = 0.4\,ms$	$K = 6.2973$ $T_i = 0.002$

The PLL of Fig. 3 is simulated in PSIM for a network frequency of 60 Hz and with the parameters of Table I. The synchronism error is determined as the difference between ($\theta_g - \theta$), which is measured in degrees sexagesimals and is shown in Fig. 6. It is observed that the maximum overshoot is around 13° and the establishment time is around 6 ms, which is a good result.

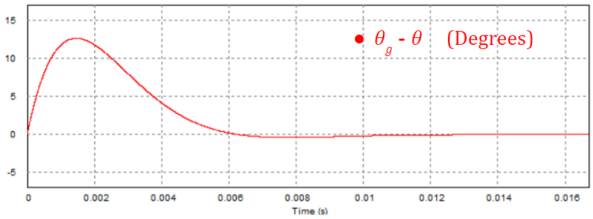

Fig. 6. Dynamics of the PLL synchronization error in PSIM.

B. DC-Link control

En x se muestra To design the V_{dc} control, the I_g control is first designed, whose transfer function is expressed in (4) and is applied in both loop d and loop q.

$$G_{LCL}(s) = \frac{R_d C_f s + 1}{C_f L_1 L_2 s^3 + R_d C_f (L_1 + L_2) s^2 + (L_1 + L_2) s} \quad (4)$$

The parameters of the LCL filter are shown in Table II.

Table II. Parameters of $G_{LCL}(s)$.

Parameter	Notation	Value
Inductance on the IGBT side	L_1	1000 µH
Grid side inductance	L_2	100 µH
Filter capacitance	C_f	15 µF
Damping resistance	R_d	0.7878 Ω

Using classical control methods such as Ziegler-Nichols, the PI control parameters for $G_{LCL}(s)$, are tuned; such values are shown in Table III.

Table III. Current loop PI control parameters

Parameter	Value
Proportional gain	4.77
Integral time	0.183 x 10^{-3}

For the DC-Link voltage control (V_{dc}), the transfer function (5) is deduced after applying Kirchhoff's first law to the DC-Link capacitance in Fig. 2.

$$G_{dc}(s) = -\frac{m}{Cs} \quad (5)$$

The parameters of $G_{dc}(s)$ are shown in Table IV.

Table IV. DC-Link PI Control Parameters.

Parameter	Notation	Value
Modulation index	m	0.8
DC-Link Capacitance	C	360 µH

Since the dynamics of the I_g loop must be faster than that of the V_{dc} loop. The parameters of the PI control of the V_{dc} loop are designed by bode. Such parameters are shown in Table V.

Table V. DC-Link voltage PI control parameters.

Parameter	Value
Proportional gain	-0.531
Integral time	0.0796

In steady state $V^*_{dc} = 450\,V$ and $I_{dc} = 10\,A$. If I_{dc} is increased by one step to 16 A, the dynamics of V_{dc} is observed in Fig. 7.

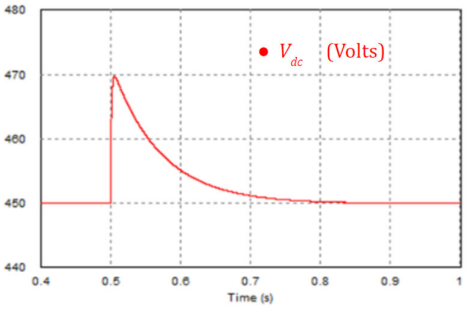

Fig. 7. Variation of the DC bus voltage due to an increase in photovoltaic panel current from 10 A to 16 A in PSIM.

3. VSI with VI capability

A. Virtual Inertia

Fig. 8 shows the control loop for supplying virtual inertia. Maintaining a desired nominal frequency (f^*) is assigned and the estimated frequency (f') is obtained by an FLL, which will be discussed later. The principle is based on a proportional control, which varies V_{dc} with a variation of f, imitating the inertia of an SG. In (6) the proportional gain K_{wv} is established by considering the maximum deviations of V_{dc} and f. In (7) the proportional gain in the system per unit K_{wv_pu} is shown.

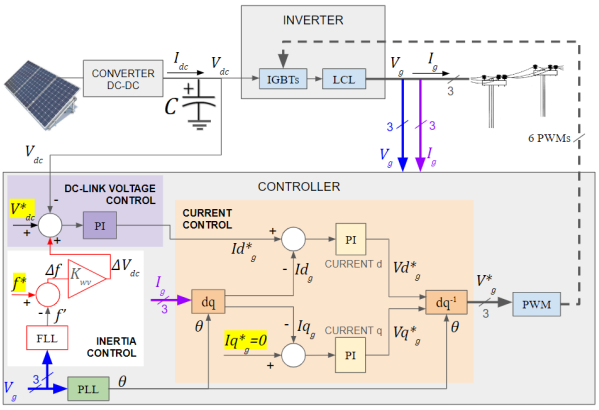

Fig. 8. VSI con VI con estimación de frecuencia mediante un FLL.

$$K_{wv} = \frac{\Delta V_{dc\_max}}{\Delta f_{max}} \quad (6)$$

$$K_{wv\_pu} = \frac{\Delta V_{dc\_max}/V^*_{dc}}{\Delta f_{max}/f^*} \quad (7)$$

Table VI shows the nominal, minimum and maximum values for the VSI design with VI in Fig. 8. The value of K_{wv} and K_{wv_pu} are obtained from (6) and (7), respectively. The inertia coefficient of the DC-Link is determined by (8) and after applying (9) a virtual inertia coefficient H_P = 5.04 s is obtained, which is a high value and comparable to the inertia of a large synchronous generator [4].

$$H_C = \frac{CV_{dc}^2}{2VA_{rated}} \quad (8)$$

$$H_P = H_C K_{wv\_pu} \quad (9)$$

Table VI. Parameters and nominal values of the VSI with VI capability.

Description	Notation	Value
Desired DC-Link nominal voltage	V^*_{dc}	450 V
Maximum DC-Link voltage deviation	ΔV_{dc_max}	55 V
DC-Link Capacitance	C	2.2 mF
Desired nominal frequency	ω^*	60 Hz
Maximum frequency deviation	Δf_{max}	0.36 Hz
Rated power	VA_{rated}	0.9 kW
Frequency control proportional gain // (per unit)	K_{wv} // K_{wv_pu}	152.78 // 20.37
Virtual inertia coefficient	H_P	5.04 s

It must be kept in mind that a VSI with VI requires increasing C (see Table VI and Table IV) and the VI components must support more power, which requires greater sizing of electronic components. This is the cost of a VSI with VI. The dynamics of the virtual inertia supply depends on the design of the previously designed control loops and a good grid frequency estimation. In this paper, the frequency estimation by PLL and by FLL is compared, for the supply of virtual inertia. Fig. 8 shows the use of an FLL for frequency estimation, which will be discussed in the next section.

B. FLL design

The FLL of Fig. 9 is a frequency estimator of a noisy single-phase sinusoidal signal (v) and works together with an adaptive filter based on a second-order integrator (AF-SOGI). Therefore, you not only get the estimated frequency (f') but you also get an estimated or filtered sinusoidal signal (v'). AF-SOGI takes advantage of the estimated frequency in rad/s (ω') to obtain v'. For its part, the FLL takes advantage of the estimation error of the sinusoidal signal (ε_v) the quadrature of the estimated sinusoidal signal (qv') and v' to obtain ω'.

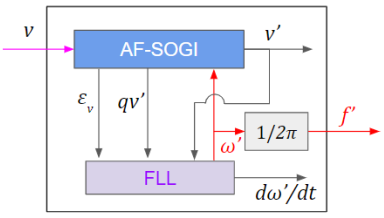

Fig. 9. AF-SOGI with FLL.

La Fig. 10 shows in detail what is shown in Fig. 9 whose structure of the FLL is quite non-linear, in [5] it is analyzed in detail. A feed forward frequency (ω_{ff}) is added to the estimated frequency, since the FLL design involves more than one linearization around the nominal frequency of 377 rad/s (60 Hz). Setting ω_{ff} = 377 rad /s, is necessary to start close to the operating point at which it has been linearized and not lose stability at the beginning.

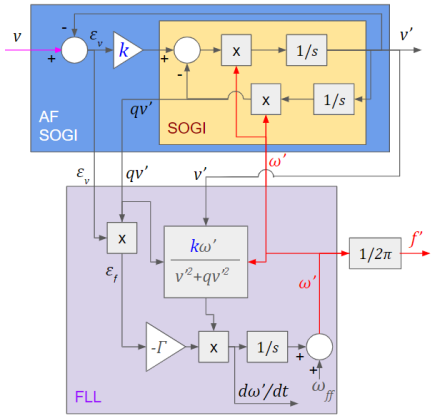

Fig. 10. AF-SOGI with FLL detailed.

The designed gains of AF-SOGI with FLL for a frequency of 60 Hz are shown in Table VII.

Table VII. AF-SOGI with FLL gains

Notation	Description	Value
k	AF-SOGI gain	1.4
Γ	FLL gain	50

In the case of frequency estimation of a three-phase signal, two AF-SOGI and one FLL are used, in addition to using the $\alpha\beta$ transform to decompose the three-phase signal, in this case it would be the grid voltage (V_g). Certain compositions of the α and β signals are necessary to enter the FLL, as shown in Fig. 11. However, the gains of the AF-SOGI and the FLL maintain the values designed in the single-phase analysis (see Table VII).

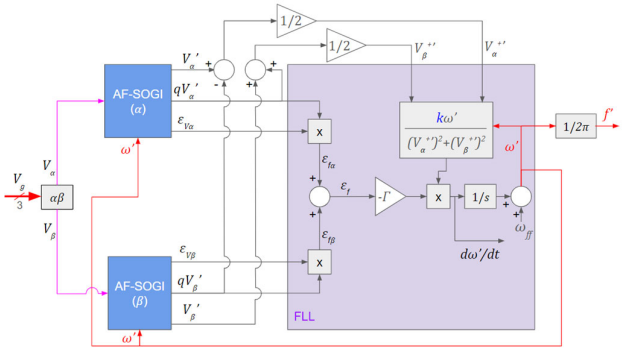

Fig. 11. Double AF-SOGI with FLL.

4. FLL versus PLL

A. Approach FLL

The Double AF-SOGI with FLL of Fig. 11 is embedded in the FLL block of Fig. 8. To test the virtual inertia supply, the grid frequency (f) is forced to be contaminated with noise white 0.02 Hz and has a step type decay from 60 Hz to 59.7 Hz. Fig. 12 (a) shows f and the estimated frequency (f'), noting a quite acceptable dynamics for frequency estimation. During virtual inertia supply V_{dc} decreases as shown in Fig. 12 (b). While Fig. 12 (c) shows that the power injected into the grid has a power hump during the transition, whose peak reaches approximately 3.2 kW (more than triple the nominal power of 0.9 kW). Although this peak power is very high for the

nominal power of the inverter, it must be taken into account that f in Fig. 12 (a) has a step type change, which in real conditions is not possible since the rate of change of frecuency (RoCoF) is infinite at the beginning of the transition. However, for later reasons of comparison between the FLL and the PLL, this condition of f is maintained.

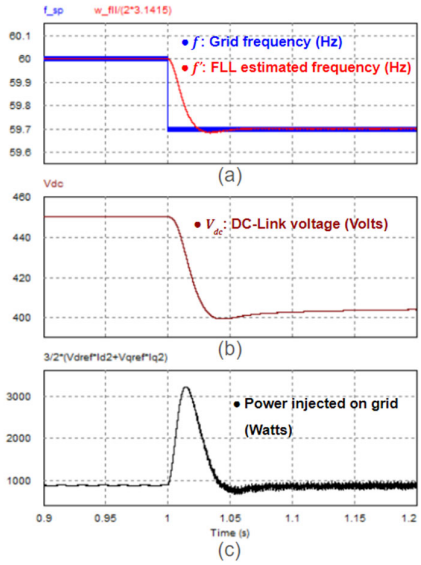

Fig. 12. Inertia emulation with FLL. (a) Frequency estimation dynamics, (b) DC-Link Voltage Drop, (c) Power injected into the grid.

Fig. 13 shows the three-phase current injected into the grid (I_g) during the virtual inertia supply. Fig. 13 and Fig. 12 (c) show distortion after the transition. The distortion is because the mains frequency has been forced to be 0.3 Hz away from its nominal value (60 Hz). Such a value is high considering the international standards allowed for frequency deviation [3]. However, it is considered for testing. Keep in mind that in the design of the control loops it has been linearized on several occasions around 60 Hz, for this reason stability is lost if the frequency moves away from this value. On the other hand, it will be seen later that the quality of the frequency estimation also influences the distortion after the supply of virtual inertia.

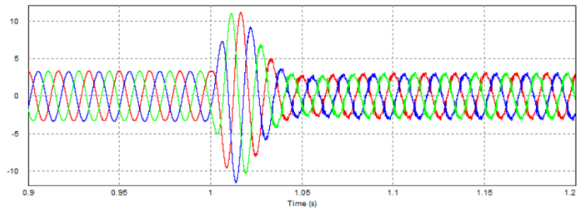

Fig. 13. VI response for a grid frequency drop of 0.3 Hz

Fig. 14 shows the dynamics of I_g for a frequency drop of 0.1 Hz, noting that the distortion is negligible in this case.

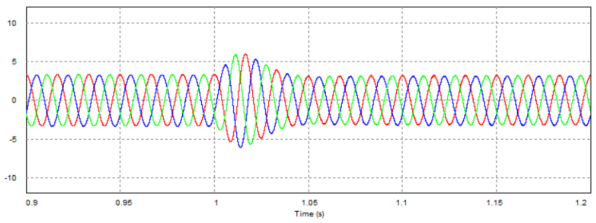

Fig. 14. VI response for a grid frequency drop of 0.1 Hz

B. *Approach PLL*

The network frequency can be estimated from both the FLL in Fig. 11 and the PLL in Fig. 3. In the case of the PLL, the frequency is obtained by extracting the signal behind the integrator, which makes it more susceptible to noise or disturbances. Fig. 15 shows the frequency estimation of the FLL and the PLL in the event of a step-type drop in the grid frequency from 60 Hz to 59.7 Hz, in which 0.02 Hz of white noise has been added (as in the previous analysis).

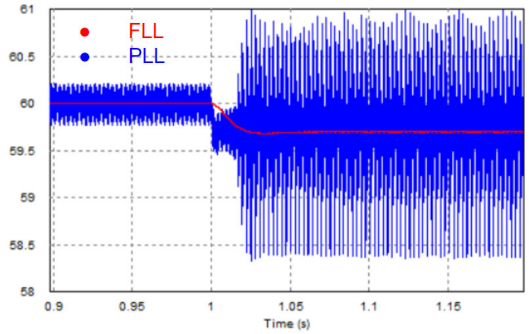

Fig. 15. Frequency estimation of FLL and PLL.

Due to the amplification of noise in the PLL frequency estimation, it is appropriate to add a first-order low-pass filter with time constant τ. Which has been considered in Fig. 16 for inertia emulation. Unlike Fig. 8, the frequency is estimated using the PLL designed in section 2.

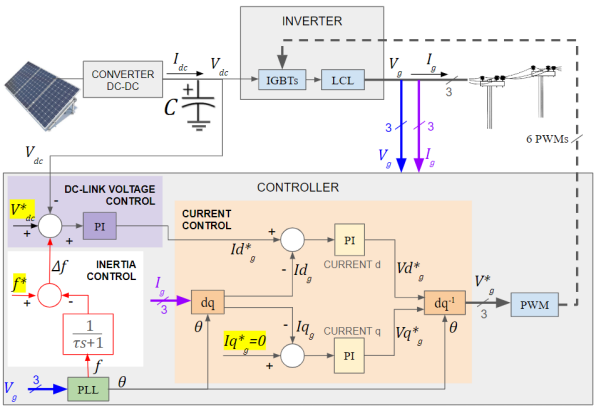

Fig. 16. VSI with VI with frequency estimation using a PLL.

Fig. 17 compares the frequency estimate obtained by the FLL with the PLL, applying low-pass filters to the output of the PLL at the frequencies of 5 Hz, 10 Hz and 20 Hz.

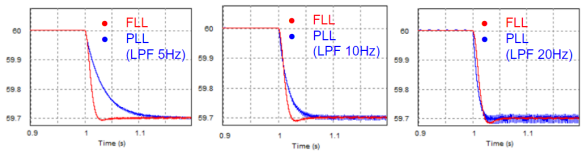

Fig. 17. Comparison between FLL and PLL with low pass filter at frequencies of 5Hz, 10 Hz and 20 Hz, for a 0.3 Hz drop on grid.

Fig. 18 shows the DC-Link voltage (V_{dc}) and the power injected into the grid (P_g), using a PLL with a low-pass filter at the frequencies shown in Fig. 17. It is observed that for low bandwidth band the dynamics is slow both in the frequency estimation and in V_{dc}, in addition, there is a lower power peak during the supply of virtual inertia and a low distortion after the transition. On the other hand, for a greater bandwidth the dynamics are faster both in the frequency estimation and in V_{dc}, in addition there is a greater peak power during the supply of virtual inertia and a greater distortion after the transition.

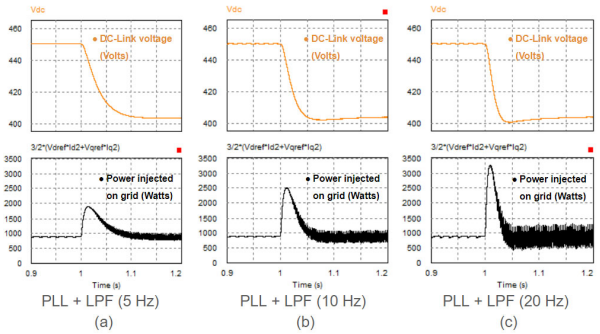

Fig. 18. DC-Link voltage and Power injected into the grid, using PLL with FPL: (a) 5 Hz, (b) 10 Hz y (c) 20 Hz.

The result obtained in Fig. 18 (c) is similar to that obtained with the FLL Fig. 12. However, the distortion is larger after the transition, which is undesirable. Taking into account that the virtual inertia supply is the same in the 3 cases of Fig. 18, since the DC-Link voltage in the end stabilizes at the same value, which is equivalent to saying that the hump area in the 3 cases is the same, since the same energy is injected during the inertia supply. Therefore, the best case is to use a PLL with 5 Hz LPF, since it delivers the same virtual inertia, but without a high peak power and with less distortion after the transition.

5. Conclusion

The main conclusion of this paper is that the FLL can have a more precise and stable estimation of the grid frequency than that of the PLL, even the PLL needs a low-pass filter for an appropriate estimation of the frequency. However, inertial dynamics are relatively slow, so fast frequency estimation is not needed. For this reason, a PLL with an appropriate low-pass filter will provide the same virtual inertia as the FLL, but with a lower peak power. This result is good, since it implies less computational cost and less resizing of the inverter. It should be considered that the conclusion established is for the case of a step frequency drop, which is not realistic. An analysis with a ramp-type frequency drop, to resemble more real conditions or add a filter to the FLL or establish specific requirements for the supply of virtual inertia, can change the conclusion presented.

Acknowledgement

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References

[1] COES, "COES," [Online]. Available: https://www.coes.org.pe/Portal/home/. [Accessed 03 04 2024].

[2] Kundur, Power System Stability and Control, Palo Alto, California: McGraw-Hill, 1993.

[3] J. Fang, H. Li, Y. Tang and F. Blaabjerg, "On the Inertia of Future More-Electronics," *IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS,* vol. 7, no. 4, pp. 2130-2146, 2019.

[4] A. Otto Villa, "Dimensionamiento Preliminar de Generadores Sincrónicos de Eje Vertical," *Trilogía de Ciencia,Tecnología y Sociedad,* pp. 115-122, 2012.

[5] P. Rodr ıguez, A. Luna, R. S. Muñoz-Aguilar, I. Etxeberria-Otadui, R. Teodorescu and F. Blaabjerg, "A Stationary Reference Frame Grid Synchronization System for Three-Phase Grid-Connected Power Converters Under Adverse Grid Conditions," *IEEE TRANSACTIONS ON POWER ELECTRONICS,* vol. 27, no. 1, pp. 99-112, 2012.

[6] ENTSO-E, "Rate of Change of Frequency," Avenue de Cortenbergh 100, 2018.

[7] X. Ruan, X. Wang, D. Pan, D. Yang, W. Li and C. Bao, Control Techniques for LCL-Type Grid-Connected Inverters, Beijing: Springer, 2018.

[8] J. Fang, H. Li, Y. Tang and F. Blaabjerg, "Distributed Power System Virtual Inertia Implemented by Grid-Connected Power Converters," *IEEE TRANSACTIONS ON POWER ELECTRONICS,* vol. 33, no. 10, pp. 8488-8499, 2018.

[9] J. Fang, R. Zhang, H. Li and Y. Tang, "Frequency Derivative-Based Inertia Enhancement by Grid-Connected Power Converters With a Frequency-Locked-Loop," *IEEE TRANSACTIONS ON SMART GRID,* vol. 10, no. 5, pp. 4918-4927, 2019.

[10] B. Widrow, J. Glover, J. McCool, J. Kaunitz, C. Williams, R. Hearn, J. Zeidler, E. Dong and R. Goodlin, "Adaptive Noise Cancelling: Principles and Applications," *PROCEEDINGS OF THE IEEE,,* vol. 63, no. 12, pp. 1692-1716, 1975.

[11] P. Rodriguez, A. Luna, I. Candela, R. Teodorescu and F. Blaabjerg, "Grid Synchronization of Power Converters using Multiple Second Order Generalized Integrators," in *34th Annual Conference of IEEE Industrial Electronics*, Orlando, FL, USA, 2008.