

Modular Multilevel Converter Control Strategy with Fault Tolerance

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Abstract. The Modular Multilevel Converter (MMC) technology has recently emerged in VSC-HVDC applications where it demonstrated higher efficiency and fault tolerance compared to the classical 2-level topology. Due to the ability of MMC to connect to HV levels, MMC can be also used in transformerless STATCOM and large wind turbines. In this paper, a control and communication strategy have been developed to accommodate tolerant module failure and capacitor voltage unbalance. A downscaled prototype converter has been built in order to validate and investigate the control strategy, and also test the proposed communication infrastructure based on Industrial Ethernet.

Keywords

MMC, HVDC, Converter, Transformerless wind turbine,

1. Introduction

Wind energy penetration is growing and the size of wind turbines also, especially for offshore applications where turbines in the range of 3-6 MW are now tested [1]. In order to comply with the more demanding grid codes in some countries with high wind power penetration (Denmark, Germany, Spain, UK, etc.) full-scale back-to-back (BTB) converters are more and more used in [2]. The MMC concept appears to be a promising technology recently introduced for high-voltage high power applications, due to the increased efficiency, redundancy provision and high quality voltage output with reduced dv/dt and output filter requirements [3-4]. Due to these advantages, the MMC is being now used by most of the VSC-HVDC manufacturers like ABB (HVDC-Light), Siemens (HVDC-Plus) and Alstom (HVDC-MaxSine) and also in STATCOM applications (Siemens SVC-Plus) and large wind turbines directly connected to MV levels [5].

2. Design and modeling

In the following, we consider an MMC converter applied to a 10 MW/20 kV transformerless wind turbine. The main data is shown in TABLE I.

TABLE I. INITIAL REQUIREMENTS

Description	Abbreviation	Value
DC-link voltage	V_{dc}	36 kV
Output AC RMS voltage	V_{L-L}	20 kV
Rated active power	P_N	10 MW
Power factor	$\cos \varphi$	± 0.9
Number of sub-modules per arm	n	13
Sub-module nominal voltage	$V_{SM,nom}$	2.77 kV
Number of voltage levels	-	14

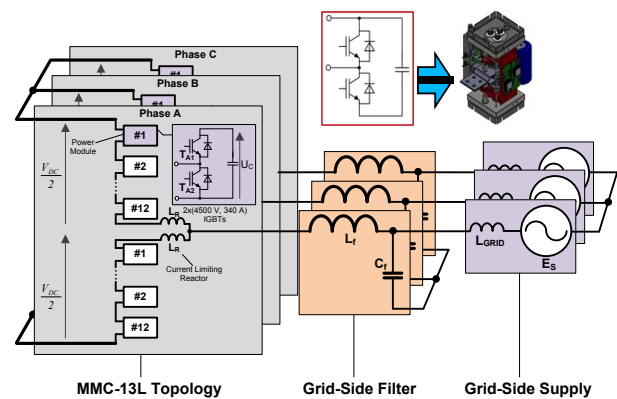


Figure 1: Three Phase MMC for TL Wind Turbine

One redundant sub-module was placed in each arm. This redundant module participates in the operation but in case of failure it can be bypassed and the converter operation can continue with acceptable quality output voltage. The remaining sub-modules are tolerant to the 8% increase of the voltage.

Considering the operation principle of the MMC, each capacitor has to be rated to the DC-link voltage level which is divided by the number of sub-modules in one arm, taking into account safety and redundancy margins. Another aspect that should be taken into account is the storage capability of the capacitor. This means that it has to be able to provide the rated power during transients in the DC link.

Arm inductors have to be selected based on the fault current rise-rate limitation criterion. The inductors are series connected, and this can reduce both internal and external fault currents therefore preventing the damage of the equipment under test [6].

A. CAPACITOR DIMENSIONING

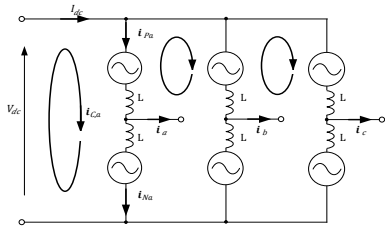


Figure 2: Representation of circulating currents

If the converter arm consists of n sub-modules, the energy change in one sub-module is given by [7]:

$$\Delta W_{source}(k) = \frac{2}{3} \cdot \frac{S}{k \cdot \omega_N \cdot n} \cdot \left(1 - \left(\frac{k \cdot \cos \varphi}{2} \right)^2 \right)^{\frac{3}{2}} \quad (1)$$

where S is the apparent power of the converter, k is the voltage modulation index, ω_N is the output angular frequency, n is the number of sub-modules per arm and φ is the output angular frequency.

Assuming that a sub-module capacitor has a relative voltage ripple ($\pm \varepsilon$) around the nominal voltage for which the capacitor is designed, the energy of the capacitor can be expressed as:

$$W_c(V_{SM,nom}) = \frac{1}{2} \cdot C_{SM} \cdot V_{SM,nom}^2 = \frac{1}{4 \cdot \varepsilon} \cdot \Delta W_{SM} \quad (2)$$

From equation (2), the sub-module capacitance (C_{SM}) at any desired voltage ripple ($0 < \varepsilon < 1$) can be derived as:

$$C_{SM} = \frac{\Delta W_{SM}}{2 \cdot \varepsilon \cdot V_{SM,nom}^2} \quad (3)$$

In case of the designed converter: $C_{SM} = 1 \text{ mF}$ (4)

B. ARM INDUCTOR DIMENSIONING

When selecting the arm inductors which limit the fault currents rise-rates, the most critical faults have to be considered; i.e. short circuit between the DC link terminals. In the first instant of fault, the sum of the voltage over the inserted capacitors is equal to the DC link voltage. The voltage drop over the arm inductors, according to Kirchhoff's voltage law, is [8]:

$$L \frac{di_{Pa}}{dt} + L \frac{di_{Na}}{dt} - V_{dc} = 0 \quad (5)$$

where L is the arm inductance, I_{Pa} and I_{Na} are the positive and negative arm currents and V_{dc} is the DC-link voltage. For short transients, both arm currents are assumed to be equal, so equation (5) can be rewritten as [8]:

$$\alpha = \frac{di_{Pa}}{dt} = \frac{di_{Na}}{dt} = \frac{V_{dc}}{2L} \quad (6)$$

Where α is the rise-rate of the fault current in kA/s. Furthermore, in equation (6), the arm inductor depending on the current rise rate can be expressed as:

$$L = \frac{V_{dc}}{2\alpha} = 0.27 \text{ mH} \quad (7)$$

3. Capacitor Balancing Method

During the operation, sub-module capacitors experience an unequal voltage share due to the operation principal. This affects the output voltage waveform by lowering the efficiency and quality indicators of the converter. There are several possibilities to achieve equal voltage over the arm capacitors without having external voltage sources. This is based on the sorting of the sub-modules by choosing wherever a module has to be in ON-state or OFF-state for each operating cycle [9]. The sorting criteria is based on:

- direction of the arm current;
- capacitor voltage.

The sorting algorithm will switch on the capacitors with the lowest voltages when the current flow is positive and vice versa for negative current. This method ensures that n capacitors in each phase leg are sharing the DC link voltage at all the time. In consequence a smaller arm inductance is required to suppress the circulating currents [10]. This results in balancing currents circulating between the legs as shown in Figure 2. Due to the symmetric structure of the converter, phase A will be used as an example. Figure 2 shows the positive and negative arm currents, i_{Pa} and i_{Na} respectively. The circulating current along the phase A loop i_{Ca} is used to represent the arm current. The load current of the phase A is noted with i_a .

$$L \frac{di_{Pa}}{dt} + L \frac{di_{Na}}{dt} - V_{dc} = 0 \quad (8)$$

Figure 3 presents the implementation of the sub-module

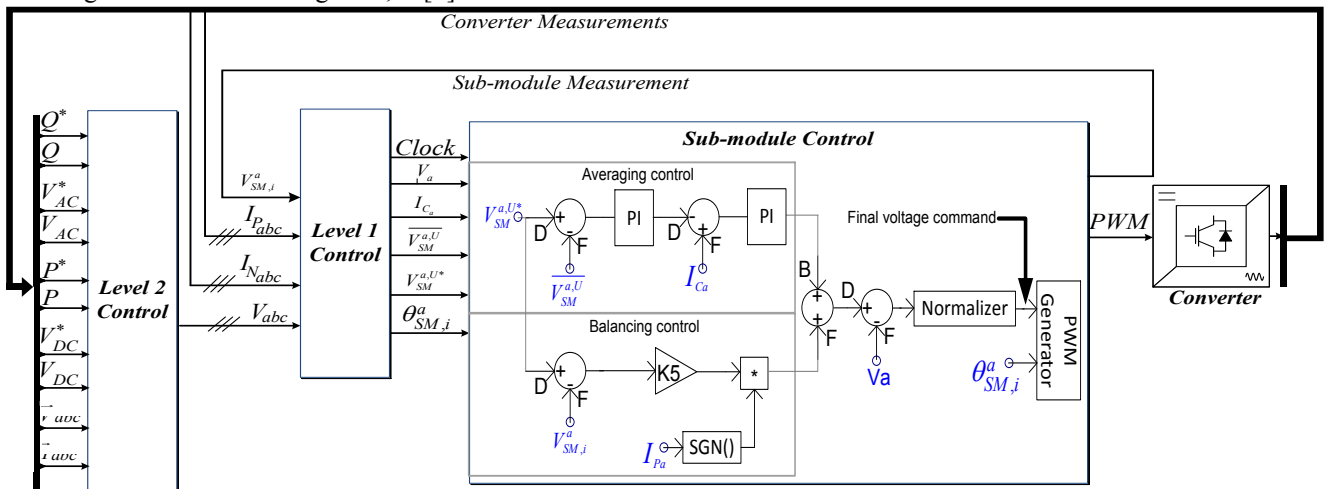


Figure 3: Implementation of converter control with focus on a sub-module control from the upper arm in phase a

balancing control and its integration with the high level control. From the high level 1 control a voltage reference for the entire phase A is given (V_a) which will be included in the balancing controller. The balancing controller shown is specific to any sub-module in the upper arms of phase A. The level 1 controller measures the positive ($I_{P_{abc}}$) and the negative ($I_{N_{abc}}$) arms currents, and then send an mean of the phase currents (I_{C_a}) to each sub-module to be used in the averaging controller. The sub-module also receives a capacitor voltage reference ($V_{SM}^{a,U*}$) identical to the entire arm(U=upper arm) in the phase A which needs to be followed and an average of the capacitors voltages ($\overline{V_{SM}^{a,U}}$) in the entire arm of the phase. From the capacitor voltage reference, the balancing controller subtracts its instantaneous value and multiplies it with the sign of the current in the arm, in this case the upper one (I_{P_a}). The signals from the balancing controller are added up together and then normalized before being fed into a PWM generator. The PWM generator receives a phase displacement angle ($\theta_{SM,i}^a$) specific to its position in the arm (i) in order to generate the PWM for the sub-module. It can be observed in Figure 4 that the sub-module balancing control forces the sub-module voltages to reach an equal distribution independently on the particular phase shift of the triangular carrier in case of failure and bypassing of one SM with a slight increase in the voltage.

4. Loss Analysis

The current in the devices is spread unequally in a SM; the lower switch and the upper diode conduct a higher amount of current. The average positive and negative arm currents have to be obtained in order to calculate the switching losses. They can be derived analytically and can be confirmed by the simulations. Simulations scenarios show that for different switching frequencies and arm inductors different efficiencies can be achieved (see Table II.). For this case 260 Hz has been selected leading to a high total efficiency of 98.5%

Table II. – Efficiency vs Switching frequency for 10MW/20 kV MMC

		Arm inductor value				Total eff.%	
		1 mH	2 mH	3 mH	5 mH		
Switching frequency	260 Hz	Cond. losses, kW	79.56	78.23	77.92	78.70	98.5
		Sw. losses, kW	37.066				
		Total losses, kW	116.6	115.3	114.9	115.6	
	360 Hz	Cond. losses, kW	78.94	77.06	76.99	77.69	
		Sw. losses, kW	51.322				
		Total losses, kW	130.3	128.4	128.3	129.0	

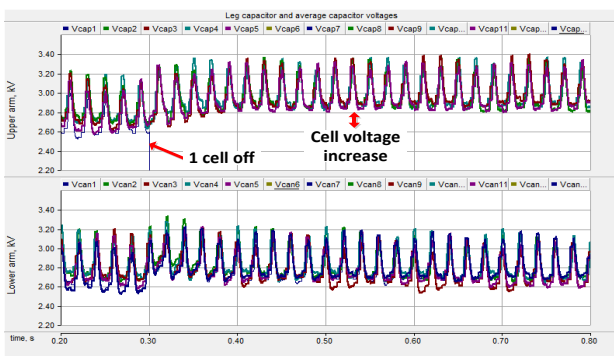


Figure 4: Capacitor voltage balancing after 1 SM failure

5. Distributed control

Figure 5 shows the data exchange between a master and a slave. The master send a global broadcast to the entire converter in terms of: modulation frequency, modulation index, PI controller's gains, operation mode (converter/inverter) and an enable command. This global broadcast will be resent only when one of the values needs to be changed.

A leg broadcast is sent separately to each leg to set the phase number. This value (0-3) will be multiplied with the angle difference between each phase in order to create the 3 sinusoidal references for the PWM. This value will be updated only when it is needed. The circulating currents will be averaged from the measurements done by the master and sent to each slave from the leg in order to be used by the balancing controller.

An arm broadcast is sent with the number of sub-modules from a leg, the phase displacement angle, the reference capacitor voltage and the average from the last update cycle. The phase displacement will be used by the slaves in order to ensure proper distribution of the triangular waves. The capacitors average value will be updated during each cycle, while the other will only be update when reconfiguration is needed.

Finally each sub-module will receive an individual message containing its position in the arm, in order to ensure proper distribution of the modulation.

In turn, each sub-module will communicate each cycle its capacitor voltage, and its status. This will ensure than the communication won't be interrupted and that no sub-module is faulty and disrupt the proper operation.

6. Communication Technology

Industrial Ethernet has been developed and takes advantage of well-established Ethernet [11] (speed up to Gbs, large number of nodes, and low cost hardware). There are different industrial Ethernet implementations available for complex drives systems and other control applications which require high bandwidth, fast updates

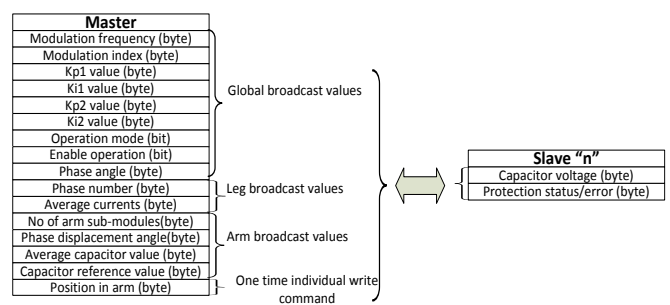


Figure 5: Variable communication

times and good clock synchronization. There are different implementations already on the market, most of them proprietary and hard to interconnect. Some implementations have been released as open source: ProfiNet [12], EtherCAT [13], etc. Due to its better performance [14] for this protocol EtherCAT was chosen as a communication solution.

EtherCAT is an open source protocol currently managed by the EtherCAT Group (ETG) [13]. It uses standard Ethernet frames as defined by IEEE 803.2 [11]. In theory Master and Slave can be implemented by using standard

off the shelf interfaces (PHY and MAC), but in order to improve the package forwarding delays the slaves are implemented on hardware like FPGAs or ASICs. The Master on the other hand can be implemented on any off the shelf hardware, without any special requirements. A typical EtherCAT network consists of at least one master unit and up to a theoretical 65535 slaves. The communication speed is limited to 100Mbps, and although in theory it could go up to gigabit speeds, however, no existing slave hardware can handle that high speed.

At the moment there is a wide variety of master code implementations to suit the needs for the industry. The slave code has been implemented on a large number of FPGAs and ASICs, giving the user flexibility in choosing the optimum solution. A typical EtherCAT telegram and its integration into an Ethernet frame is presented in Figure 6.

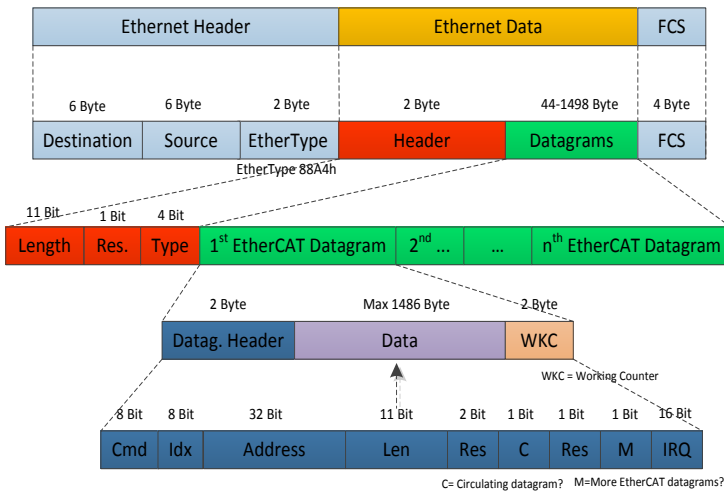


Figure 6 - Ethernet frame with EtherCAT data structure

All the EtherCAT telegrams are initiated by the master. As the telegrams pass through the slaves hardware, each slave reads the data addressed to it and writes the requested data in its assigned position inside the telegram. This normally translates in propagation delays under 500ns, depending on the used implementation [14]. More than one slave can be addressed in a telegram. This mechanism provides a better bandwidth usage compared to traditional Ethernet frames, due to the minimum frame size. The communication cycles can be defined in the master, and can be as low as 50 μ s. Each cycle can send more than one telegram, and in case the update time is shorter than the time needed for the telegram to travel back, the master program will be signaled and the refresh time will be increased in order to accommodate the traveling time.

To facilitate the communication, each EtherCAT slave controller (ESC) has a 3 buffer memory. This ensures that the latest information will always be present between the telegram and the micro-controller (μ C), in case the update times of one of them is faster than the other. As soon as either the EtherCAT processing unit or the μ C starts writing the first bit in one of the 3 buffers, that buffer gets locked until the last bit is written. At that point the buffer is available for reading. This is handled automatically by the ESC.

EtherCAT offers its own implementation of IEEE 1588 [15]. The clock synchronization is implemented in the

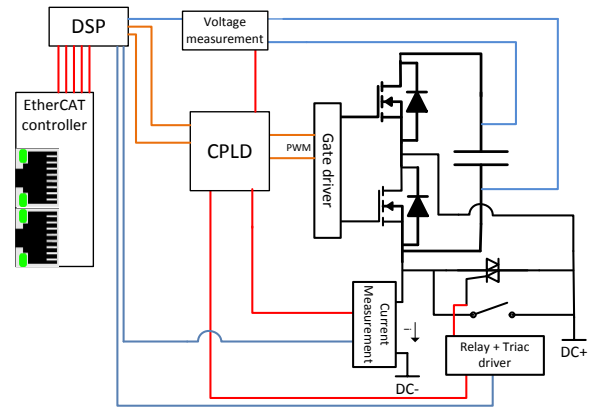


Figure 7 - Sub-module construction

Red: logical signals; blue: analog signals; orange: PWM.

hardware, allowing for an accuracy of below 1 μ s (mostly determined by the clock source used by the hardware). The slave closest to the master normally is the clock master or reference clock in an EtherCAT network, and because of the use of distributed aligned clocks, they are tolerant to communication faults and delays compared to fully synchronous communication.

Typical slaves have at least one communication port, but it can be extended up to four, allowing the network to be constructed based on any topology. The telegram is read/written as it passes from port 0 to port 3 by the EtherCAT processing unit and then forwarded to next opened port. In case port 0 is closed, as the telegram passes it, the circulating counter will be increased. If the telegram passes again through a closed port 0, the telegram will be destroyed. This is a safety feature in order to ensure, that in case of a communication failure with the master a telegram will not keep circulating in the ring and possible give erroneous commands to the slaves.

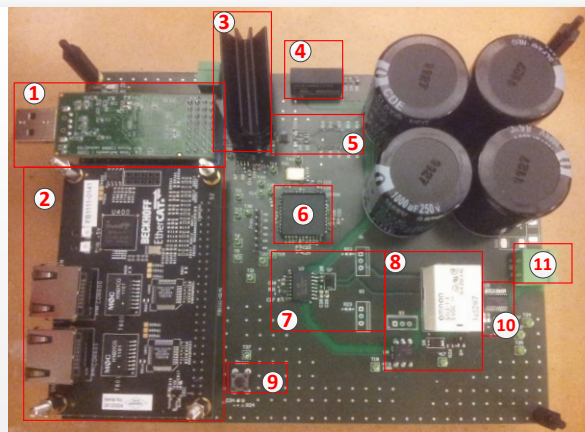
7. Reduced Scale Prototype

For the communication testing a 9 level (16 sub-modules) 10kVA 400Vac single phase MMC is constructed, supplied from a 800V DC-Link. For the control of the converter a distributed controller topology will be used, with phase-shifted triangular carrier pulse width modulation [16]. The master will decide on the modulation frequency, index and phase shift based on the number of modules connected, and the input and output voltages. In order to limit the circulating currents and the unbalance between the sub-modules capacitors, the balancing controller presented in [17] will be used.

It is composed of 8 half-bridge sub-modules per arm. The picture of one sub-module is shown in Figure 8. The used Microcontroller is a Texas Instruments TMDX28069USB. The EtherCAT communication is connected through a piggyback card with an ASIC ET1100 from Beckhoff, which is further connected to the microcontroller via 10MHz SPI bus.

The Half-bridge and capacitors are galvanic isolated from the control part of the board, allowing the high-voltage ground to float as it desires. The power on the high voltage ground is supplied through a DC/DC converter for the lower Mosfet, while for the higher Mosfet a bootstrap configuration is used. The Driving IC provides insulation of the signals and a dead-time protection of 100 μ s delay.

Figure 7 shows a simplified electrical schematic of the module. The blue wires present analog measurements, the orange lines represent the PWM, the red ones the digital signals while the black ones the power connections. DC+ and DC- are the 2 terminals of the sub-modules. The current is measured on the negative side of the capacitor, and together with the voltage measurement will be used for the balancing controller and modulation. Both measurements will also provide a digital signal for the CPLD when a dangerous situation is present (over-voltage/over-current) in order to trigger the protections. The protection is implemented using a triac and a relay across the connection terminals of the board. In case of



1- μ C
2- EtherCAT Slave Controller
3- 5V Vreg
4- Insulated DC/DC converter
5- Voltage measurement
6- CPLD
7- H-bridge with Driver
8- Bypass protection
9- Trigger button
10- Current measurement
11- H-bridge connection terminal

Figure 8: Reduced Scale prototype SM

fault the sub-module will be bypassed. The triac provides fast reaction times until the relay which closes slower, will provide a crowbar permanent connection.

In order to synchronize the Microcontrollers, the communication board provides two synchronization signals which can be configured to trigger on all the modules at the same time. These synchronization signals can be used to inform the μ C that the communication buffer holds new data. Also it can inform that new communication data should be written in the buffer in order to be read by the passing telegram in the current communication cycle.

8. Fault tolerance

As mentioned before, the MMC should continue proper operation with one or more (based on design) faulty sub-modules. Among the faults which can be handled there are: over-current due to capacitors short circuit, switching devices failure or communication failure.

a. Detection and bypassing of a sub-module in case of short-circuit or over current fault

As described in the previous section, the board has different hardware implemented protections in order to have a fast reaction time. Although dead-time is implemented in the modulation, the driving circuit is designed to not allow shoot-throughs. If one of the Mosfets will get blocked in close position, as soon as the other

Mosfet is closed, the capacitors will be short-circuited and the voltage across their terminals will drop very fast. When the DC-link is short-circuited a high current is generated which might overheat and damage the switching devices. The voltage and current is measured constantly in order to be used for the control, but at the same time also for protection. As soon as the voltage drops under a pre-defined (non-operating) voltage, which means there is a short circuit in the H-bridge, or the current increases over the nominal value for more than 100nS, the CPLD will disable the modulation. The module is bypassed by enabling the triac through an optotriac and by closing the relay. The Triac is used for its fast reaction time, but in order to limit the impact of the bypassed module, a relay will be used to permanently bypass the sub-module.

When the protection is activated, the CPLD will also signal the μ C, and at the next communication cycle the master will be informed about the bypassed module. In case the over current protection is triggered on too many modules, the master, will automatically open the circuit breaker on the DC-link, signaling a DC-link short-circuit. All this will normally happen in 2 communication cycles which should take maximum 100 microseconds.

When only one module is bypassed, the master reconfigures the rest of the sub-modules in order to compensate for the by-passed module, while the μ C from the by-passed module will try to diagnose the fault and decide if it can still participate in the modulation.

b. Detection and bypassing of sub-module in case of communication fault and online reconfiguration

Unless a message is broadcasted, each slave would normally have a datagram address directly to it. EtherCAT has different communication fault detection mechanism built inside. The most easy to use is the working counter. As the telegram leaves the master it will have a working counter (WKC) equal to "n", where "n" is the number of slaves that telegram is addressed to. Based on the CMD byte, the slave will have to read or write or read and write in that datagram or do nothing. Each time the slaves sees a datagram addressed to it, it will take the WKC and subtract 1 for a write command and 2 for a read command, if the command issued by the master was successful. When the telegram will return to the master, it will look at all the working counters and compare them to the expected values, determining if the communication was or wasn't successful with one or more slaves.

In order to achieve communication redundancy the simpler solution is to use a ring configuration as shown in Figure 9a. While the cable is intact, the same telegram is sent to both ports A and B. The telegram which leaves port A (orange) will pass through the ESC of each sub-module, and will get forwarded to the next opened port until it reaches port B of the master. The same instance of the telegram will leave port B towards port A. As it is not entering in each sub-module on the main port (port zero), it will be directly forwarded to the next opened port until it reaches port A of the master. Normally, the first slave will be chosen as reference clock.

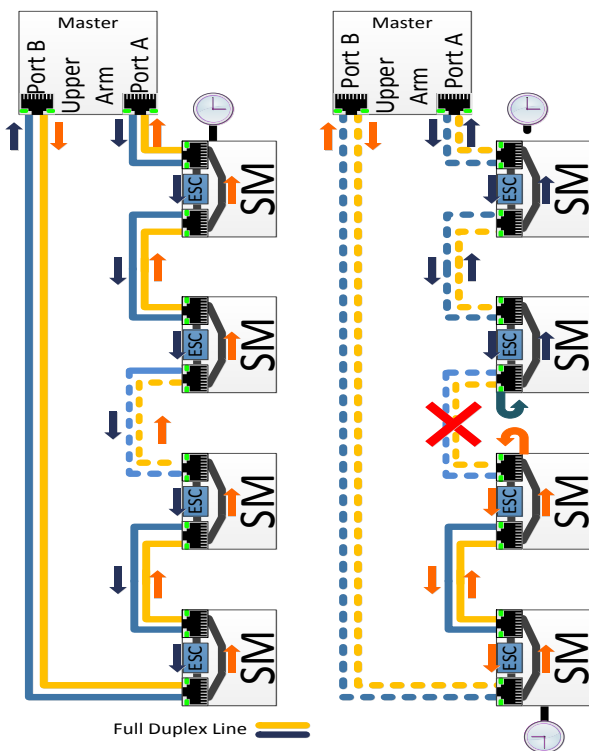


Figure 9 - Arm Redundancy arrangement(a) and reconfiguration (b)

In case of a failure (Figure 9b), the telegram which leaves port A, will be returned by the ESC of the second sub-modules as it noticed that the output port got closed by the broken cable. It will return to the master through the same port (port A). The same telegram left at the same time from port B of the master, it will get to the now closed connection port of the 3rd sub-module, and it will be automatically forwarded to the first open port (back). As it return it will pass through each ESC of the sub-modules. Both instances of the telegram should return at the same time to the master. The master will notice that each telegram has an invalid WKC, but it will try to put the 2 instances together, observing that they are forming a valid telegram. At this point the first sub-module from port B will be designed as a master clock for the newly created ring. This will permit the configuration to continue running without any problems.

The same approach will be taken in case of a sub-module failure. The only difference will be that the master will retry to send the telegram a few times to be sure that the ESC wasn't busy at the moment when the telegram passed. In case one of the sub-modules will be unable to communicate, the master will detect the error for datagram designed for that sub-module, will continue normal operation with the rest of the sub-modules, and will signal the control which sub-module is disconnected. The μC of the affected sub-module will enter into a safe state until communication is restored and will bypass the module in order to allow normal operation of the MMC.

9. Conclusions

MMC topology proves its superiority against 2-level topology in efficiency, reduced filtering requirement and fault tolerant operation. The distribute nature of this converter calls for a distributed control architecture based

on real-time communication where the SM carries the capacitor balancing task in an autonomous way. The SMs are switched at very low switching frequency (260 Hz) resulting in very high efficiency. In order to ensure a high apparent switching frequency, all SM are interleaved by providing a shift delay for the carrier. EtherCAT has been showed to be a good candidate for complying with the requirements of real-time control and especially for its ability to provide fault tolerant operation and on-line reconfiguration during SM failure and bypassing. Also it can be designed with redundancy in order to ensure communication optic fiber break tolerance. A reduced scale prototype has been built to validate the control strategy, balancing controller and communication.

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