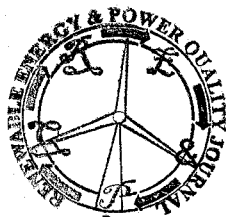


## Selective Harmonics Elimination PWM with Self-Balancing DC-link Capacitors in Five-Level Inverter



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**Abstract.** In this paper it is shown that the make use of the redundant states with selective harmonics elimination PWM in the case of multilevel inverters is possible so as to produce the required fundamental voltage while at the same time not generate higher order harmonics and balance the four  $dc$  voltage sources without additional circuitry.

### Key words

Multilevel converter, SHEPWM, Redundant states, Self-balancing.

### 1. Introduction

Multilevel inverter has been attracting extensive attention from academia as well as industry in the recent decade. They have emerged as the solution to many problems related to the traditional two-level inverter. The principal advantage is to generate a good waveform quality reducing the voltage stresses on power semiconductor devices [1][2]. So, they are very useful in high power  $ac$  applications. Several multilevel-PWM methods are developed for the two-level inverter and expanded to the multiple levels. The most popular are the multilevel carrier-based PWM derivatives. However, these techniques offer good performances using high switching frequency [3]. The SHEPWM-based method can theoretically provide various performance advantages over all the PWM methods [4][5]. These advantages include, produced the desired fundamental sinusoidal voltage while at the same time certain order harmonics are eliminated.

Otherwise, the use of this kind of inverter poses the dc-link capacitor unbalance problem [7]. Two main approaches have been proposed. 1) The use of additional passive and/or active components. 2) The manipulation of the redundant switching states.

The first solution causes an increase of system cost and additional power losses. For the second one, it is generally used in the space vector PWM.

In fact, this paper shows that the redundant states can be associated to the selective harmonics elimination PWM in order to improve more and more the performance system in term of quality signal and power losses.

### 2. NPC Five Level Inverter

The three legs of the NPC five-level inverter is shown in Fig.1. The input inverter is formed by four storage capacitors. Turning-on the suitable switches can produce five different voltage levels by leg ( $V_{dc}$ ,  $\frac{3}{4} V_{dc}$ ,  $\frac{1}{2} V_{dc}$ ,  $\frac{1}{4} V_{dc}$ , 0), as shown the stepped waveforms of fig.2.(b). The commutation of the switches permits the addition of the capacitor voltages which reach high voltage at the output.

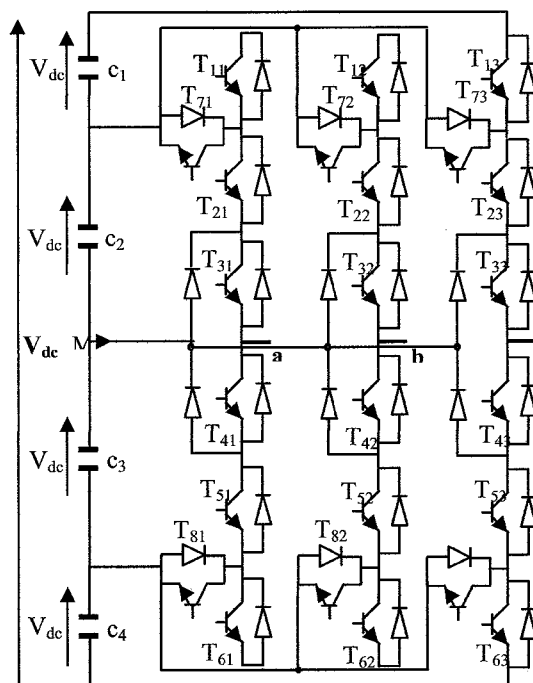


Fig.1. Schematic diagram of a NPC-5-level inverter