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FPGA Implementation of a Multiphase Space Vector Modulation for Asymmetrical Dual Three–phase AC Machines

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Abstract. Current control in conventional motor drives is normally based on controllers with sub harmonic voltage modulation techniques. Space vector modulation (SVM) for three–leg VSI and conventional motor drives has recently become a standard current control technique due to its benefits. That's why modern microcontrollers and DSPs offer internal peripheral to implement SVM technique for conventional drives. Multiphase (more than three phases) drives possess interesting advantages over conventional three–phase drives. Over the last years, topics related to the extension of control schemes to these specific drives have been covered in depth in literature. However, implementation of SVM for multiphase drives is rare due to its complexity and the specific control peripherals absence. This paper presents the FPGA implementation of a SVM strategy for a very interesting and discussed multiphase drive: the asymmetrical dual three–phase AC machine.

Keywords
Multiphase systems, current control techniques, Space Vector Modulation.

1. Introduction

Multiphase electrical drives have been recently proposed for applications where some specific advantages can be better exploited. The most important ones are: lower torque pulsations, less DC link current harmonics, higher overall system reliability and better power distribution per phase [1]. Among multiphase drives, a very interesting and discussed in the literature multiphase solution is the dual three–phase induction machine having two sets of three–phase windings spatially shifted by 30 electrical degrees with isolated neutral points (also called asymmetrical dual three–phase ac machine). The asymmetrical dual three–phase ac machine has been used in specific applications since the late 1920s [2]. For instance, in applications like electrical vehicles, the low available DC–link voltage imposes high phase currents for a three–phase drive. In this case, the dual three–phase induction machine is an interesting alternative to the conventional three–phase counterpart [3].

Current control in conventional motor drives is usually based on controllers with sub harmonic voltage modulation (PWM or Space Vector) techniques [4]. Space vector PWM technique for the dual three–phase induction machine has been recently studied [5]–[6]. However, practical implementation in the above literature using embedded systems is very harsh, complex, and expensive. For instance, a dSpace evaluation board is used in [5], with a Power PC processor to implement the current control algorithm and a Texas Instruments DSP TMS320F240 as a PWM control peripheral. These initial developments motivate us to implement the multiphase SVM strategy in a FPGA–based peripheral.

In this paper, a new hardware implementation based on a FPGA is proposed to solve the problem.

2. FPGA implementation of the multiphase SVM

The system is shown in Fig. 1. The SVM technique is implemented using a Xilinx Virtex IV FPGA, and the reference is provided by an external microcontroller. It also can be supplied by a PowerPC 405 processor which is embedded into the FPGA, and use it to implement the control algorithm.. Figure 2 presents a scheme of the FPGA implemented circuitry.

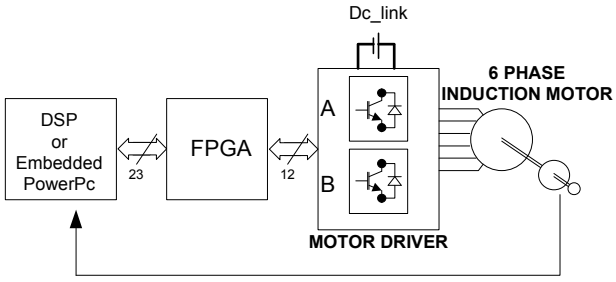

Fig. 1. System of the asymmetrical dual three–phase AC machine.

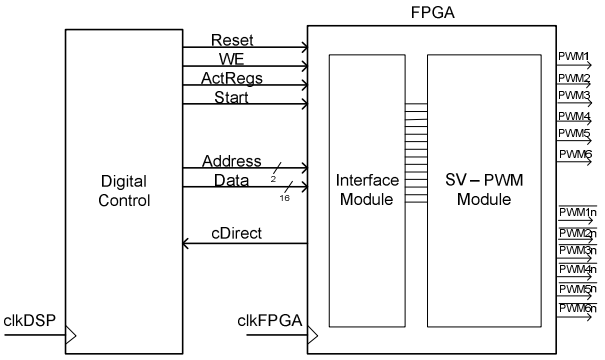

Fig. 2. Architecture of the proposed multiphase SVM control technique.

Two modules have been designed: the interface and the operational modules. The interface module allows microprocessor access and indicates the control status. The operational module, called SV–PWM module, gates de VSI legs using the following input data: the reference voltage vector in (α, β) coordinates, the sampling period (T_s), and the programmable dead time. A 23–bits data bus links both modules.

3. Obtained results

The overall design was downloaded and tested in the Xilinx ML403 Evaluation Board, using a XC4VFX12–100MHz FPGA. A picture of the experimental setup is shown in Fig. 3, while Table I summarizes the FPGA resources utilization. It can be deduced that the amount of available resources is large enough for the proposed application.

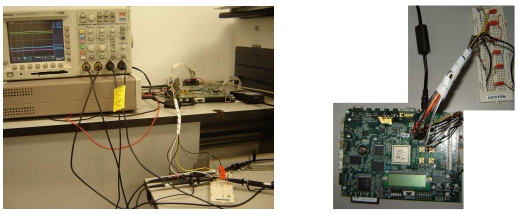

Fig 3. Pictures of the experimental setup.

A series of experimental tests were performed in order to examine the properties of the implemented circuitry. Figure 4 depicts the obtained voltage waveforms using a 50Hz stator voltage reference vector. The VSI leg pulsing outputs have been filtered using a low–pass filter to show the fundamental component. Four waveforms are shown; one corresponding to the VSI gate signal while the other are VSI gate filtered signals.

4. Conclusions

The area of multiphase induction motor drives has experienced a substantial growth in recent years. Research has been conducted worldwide and numerous interesting developments have been reported in the literature, particularly in the VSI–drive asymmetrical dual three–phase ac machine. However, the development of new microprocessor peripherals is necessary for the translation to multiphase applications of advanced digital control techniques like SVM techniques. This paper presents the design and implementation of a programmable SVM control IC for asymmetrical dual three–phase AC machines. The architecture of the FPGA implemented SVM multiphase control technique is discussed in deep, and experimental results are provided to examine the potential of the control method.

TABLE I. Device utilization summary.

Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	512	10,944	4%
Number of 4 input LUTs	1,897	10,944	17%
Logic Distribution			
Number of occupied Slices	1,091	5,472	19%
Total Number of 4 input LUTs	1,907	10,944	17%
Number used as logic	1,897		
Number of bonded IOBs	36	320	11%
Number of DSP48s	25	32	78%

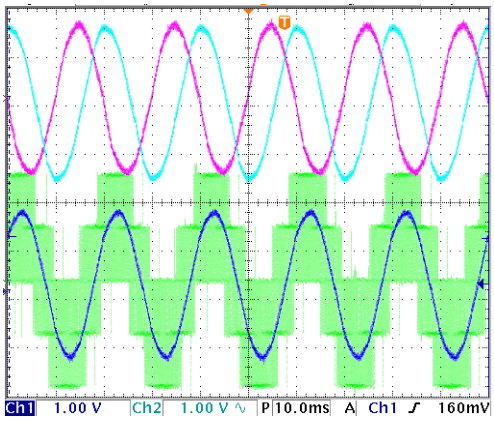

Fig. 4. Waveform experimental results for 50 Hz fundamental

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