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Simple Electrical Circuit for Large Signal Modeling of DC Microgrids

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Abstract. In previous researches, the large signal models of DC microgrids have been developed without using any time averaging technique. Thus, the results obtained from available DC microgrid large signal models have not been verified by results from their detailed models. This paper presents a suitable large signal model for DC microgrids which has the same response as control area and detailed models.

Keywords

DC Microgrid, Distributed Generation, Energy Storage, Droop Control, Hysteresis Current Control.

1. Introduction

The interest in Distributed Resources (DR), including both Distributed Generation (DG) and energy storage resources, is increasing due to their technical, economical, reliability and environmental merits. Local aggregation of DR systems and electrical loads results in a Microgrid (μG). The μG concept has provided a new paradigm for future distribution power systems. This is due to the fact that μGs are designed and controlled to meet local requirements using their own operational standards, expansion plans and power quality and reliability guidelines [1]-[4]. The infrastructure of a μG could be a DC, power frequency or high frequency AC distribution power system. The DC Microgrid (DCμG) concept provides the best solution for the μG infrastructure because it is formed simply by integrating the available DC link stages in power electronic systems which interface with modern DR systems and loads. It must be noted that the power electronic conversion systems in modern DG systems (e.g., fuel cells, microturbines, photovoltaic arrays and wind power systems), storage systems (e.g., batteries and ultracapacitors) and modern electrical loads (e.g., sensitive loads, electronic loads and AC drives) have DC power link stages. Previous researches have shown that DCμGs are preferable to both power frequency and high frequency AC μGs from technical, economical and reliability viewpoints [5]-[12].

The power electronic systems play an important role in DCμGs. Detailed and large signal modeling approaches have been used to study the power electronic systems. The detailed model of a power electronic system is derived from the variable circuit configuration of the original system by exact description of all voltage and current waveforms produced by the switching action of semiconductor switches. As a result, the detailed model is also known as switching model and can reflect both low and high frequency dynamics of the original system. The large signal model of a power electronic system is derived from its detailed model by time averaging of high frequency switching waveforms. As a result, the large signal model is also known as averaged model. The large signal model is also called behavioral model since the terminal behavior of a system obtained from its large signal model is identical to the original system at frequencies much lower than switching frequencies. In large signal modeling, nonlinearities and low frequency dynamics of the original system are maintained and only switching ripples are excluded. Thus, large signal analysis is the most effective tool for studying the system stability and control. It should be noted that the global detailed modeling approach would be too complicated with many unnecessary details. Thus, the detailed modeling is usually used as a part of a multi-level modeling approach, where detailed modeling is applied only to the subsystem of interest, and the large signal modeling is applied to the rest of the system. Consequently, the global large signal modeling of

the system is used when the system stability, subsystem interactions and controllers performance should be studied [13].

Large signal modeling of DCμGs has been studied in several researches. In [5], the large signal operation of a DCμG without storage resources and DCμG voltage measurement filters has been studied. In [9] and [10], the large signal analysis of the DCμG voltage controllers has been presented. However, the large signal models of previous researches have been developed neglecting the switching ripples without using any time averaging technique. Thus, an acceptable large signal model for DCμGs which can effectively represent the dynamic performance of the original system has not been developed in previous researches. The main goal of this paper is to develop a simple DCμG large signal model which can represent the same behavior of detailed model.

2. Operation and Control of a DCμG

The general structure of DCμG system is shown in Fig. 1.

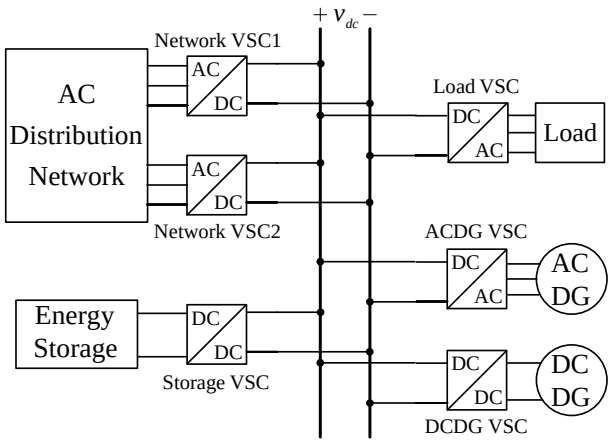

Fig. 1. General structure of DCμG

Each power electronic converter is a Voltage Source Converter (VSC) named after the subsystem it connects to the DCμG. DG resources with AC output power are named as ACDG and DG resources with DC output power are named as DCDG [7]. It is assumed that the DCμG has a lossless DC bus infrastructure formed by using a common capacitive terminal for its VSCs. Considering the requirements of the DC bus infrastructure and VSC systems, the DCμG voltage should be maintained within specified limits. In order to increase the interconnection system reliability, two network VSCs have been used [12].

Technical and economical issues generally impose the following operation and control strategies for DCμG subsystems [5]-[12]:

- In renewable energy-based DG systems such as wind or solar power generation, the main goal is to produce the maximum energy of the system to recover the installation cost.
- In fuel-based DG systems, such as fuel cells and microturbines, the costs of fuel and maintenance should be optimized.
- Storage and network VSCs regulate the DCμG voltage.
- Load VSCs should be regulated to meet its supply requirements.

In the following, three VSC regulator modules including DC Voltage Regulator (DCVR), Power Regulator (PR) and Load Voltage Regulator (LVR) modules will be presented as building blocks of the controllers of DCμG VSCs.

3. DCμG VSC Regulator Modules

A. VSC DCVR

The DC voltage droop control method has been used for DCμG VSCs, because it does not require communication systems [5]-[12]. The current-voltage droop characteristic provides a better dynamic and transient performance in comparison to power-voltage droop characteristic [6], [14]. As a result, a current-voltage droop characteristic is used in this paper. Fig. 2 shows the proposed VSC DCVR module in this paper.

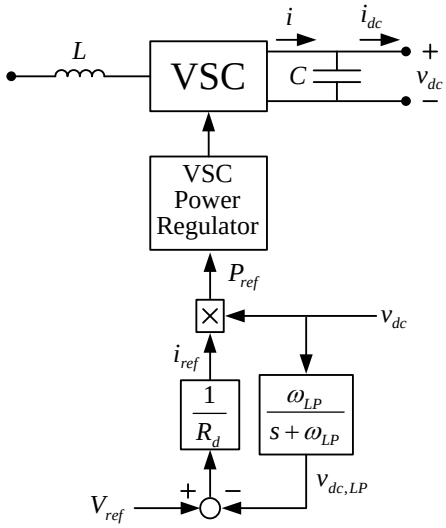

Fig. 2. Proposed VSC DCVR module

The VSC capacitor and inductor are indicated by C and L, respectively. v_{dc} is the VSC DC terminal voltage which should be controlled by the DCVR. ω_{LP} is the break-over frequency of the Low-Pass Filter (LPF). The LPF has been used to attenuate the interactions between the VSC inductive side and the DCVR system, to facilitate the controller pole-placement design [10] and to smooth the current command of the VSC [14].

The DC voltage droop characteristic is considered as follows:

$$i_{ref} = \frac{V_{ref} - v_{dc,LP}}{R_d} \quad (1)$$

where:

V_{ref} is the reference DC voltage,

R_d is the droop coefficient,

i_{ref} is the reference current for i, and

$v_{dc,LP}$ is the filtered value of v_{dc}.

The VSC reference active power is determined as follows [5]-[8]:

$$P_{ref} = v_{dc} \cdot i_{ref} \quad (2)$$

The P_{ref} is the input of the PR unit which will be discussed later. The VSC PR should provide perfect regulation at the output terminals independent of perturbations. As a result, (1) can be rewritten as follows:

$$i = \frac{V_{ref} - v_{dc,LP}}{R_d} = C\frac{dv_{dc}}{dt} + i_{dc} \quad (3)$$

In order to develop a simple electrical circuit representing the large signal model for the DCVR, the following equations have been used:

$$I_d = \frac{V_{ref}}{R_d} \quad (4)$$

and

$$L_d = \frac{R_d}{\omega_{LP}} \quad (5)$$

Substituting (4) and (5) in (3), a novel DCVR large signal model is developed as illustrated in Fig. 3.

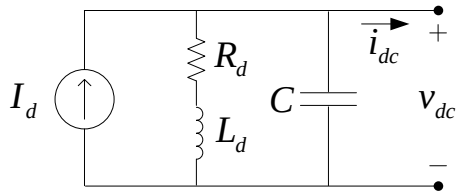

Fig. 3. Developed large signal model for VSC DCVR module

Considering Fig. 3, the steady state model of the DCVR is derived as shown in Fig. 4.

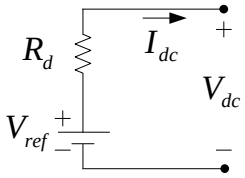

Fig. 4. Developed steady state model for VSC DCVR module

In Fig. 4, V_{dc} and I_{dc} are the steady state values of v_{dc} and i_{dc}, respectively.

To design the DCVR system, R_d and C should be calculated. The VSC inductor, L, is designed based on the PR requirements which will be discussed later. Using (1), (2) and (3), we have:

$$P = V_{dc} \cdot \left(\frac{V_{ref} - V_{dc}}{R_d}\right) = \frac{\delta \cdot (1-\delta)}{R_d} \cdot V_{ref}^2 \quad (6)$$

where:

P is the steady state active power of the VSC,

V_{dc} is the steady state value of v_{dc} and

δ is the voltage droop.

The DCVR should have an acceptable voltage droop at rated power of VSC. Thus, using (6), R_d is determined as follows:

$$R_d = \frac{\delta_n \cdot (1-\delta_n)}{P_{rated}} \cdot V_{ref}^2 \quad (7)$$

where P_{rated} is the VSC rated power and δ_n is the nominal voltage droop.

Using (3), the characteristic polynomial of the VSC DCVR is calculated as follows:

$$s^2 + \omega_{LP}s + \left(\frac{\omega_{LP}}{R_d C}\right) = s^2 + 2\xi\omega_n s + \omega_n^2 \quad (8)$$

Assuming $\xi = 0.7$ and using (7) and (8), C can be determined as follows:

$$C = \frac{2.16}{\omega_{LP}} \cdot \frac{P_{rated}}{\delta_n \cdot (1-\delta_n) \cdot V_{ref}^2} \quad (9)$$

Multiple DCVR modules are usually connected in parallel in order to control a common DC terminal voltage. Using the DCVR steady state model, the steady state model of M parallel DCVRs can be obtained as illustrated in Fig. 5.

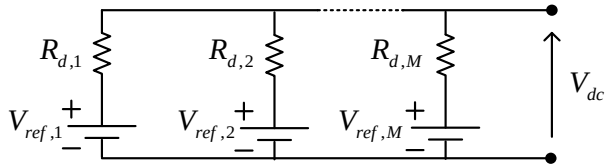

Fig. 5. Steady state model of parallel connected VSC DCVRs

In order to prevent circulating currents between the parallel DCVRs, the following condition should be assumed:

$$V_{ref,1} = V_{ref,2} = \ldots = V_{ref,M} \quad (10)$$

As a result, all parallel DCVRs will operate at the same voltage droop indicated by δ. The maximum acceptable range for DC terminal voltage variations depends on the characteristics of the DC bus and the VSCs. As a result, all parallel DCVRs are assumed to have the same nominal voltage droop indicated by δ_n. Thus, using (6), (7) and (10), we have:

$$\frac{P_1}{P_{rated,1}} = \frac{P_2}{P_{rated,2}} = ... = \frac{P_M}{P_{rated,M}} = \frac{\delta(1-\delta)}{\delta_n(1-\delta_n)} \quad (11)$$

It must be noted that each subindex number in (10) and (11) and Fig. 5 refers to its corresponding DCVR module. Equation (11) indicates equal per unit loading of the VSCs, which results in a proper power sharing of parallel connected VSC DCVRs.

B. DC/DC VSC PR

The proposed PR systems for DC/DC and AC/DC VSCs in this paper incorporate instantaneous power regulation with Hysteresis Current Control (HCC), because the instantaneous power regulation is preferable to average power based methods and the HCC has an excellent dynamic performance and is insensitivity to system parameters variations [5]-[8]. The proposed DC/DC VSC PR module is shown in Fig. 6.

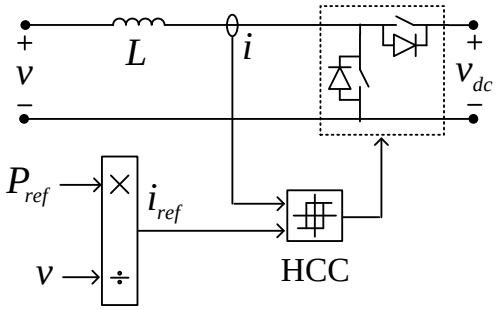

Fig. 6. Proposed DC/DC VSC PR module

The reference current is calculated as follows:

$$i_{ref} = \frac{P_{ref}}{v} \quad (12)$$

where P_{ref} is the reference active power for the DC/DC VSC PR, v indicates the DC/DC VSC inductive terminal voltage and i_{ref} is the HCC reference current.

In order to develop a suitable large signal model for the DC/DC VSC PR module, a comprehensive study of the HCC PWM is presented in the following. Analysis of the HCC systems for DC/DC buck converters is presented in [15] based on the sliding mode theory. In this paper, analysis of the HCC operation will be presented for DC/DC VSCs.

The hysteresis function is defined as follows [15]:

$$u = hyst(S, H) \quad (13)$$

where *hyst* takes an output value of 0 or 1 with a width spanning between $-H/2$ and $H/2$, where H is the hysteresis band, and S corresponds to the input signal to the hysteresis regulator, as follows:

$$S = i_{ref} - i \quad (14)$$

In the HCC active control mode, i tracks i_{ref} within the hysteresis band which defines the Active Control Manifold (ACM) to which the system state converges. The ACM is characterized by the following equation:

$$S = i_{ref} - i = 0 \quad (15)$$

The ACM does not extend globally, because the control variable u is limited. Consequently, the conditions for (15) can be calculated by applying the invariability condition, as follows:

$$\frac{dS}{dt} = \frac{di_{ref}}{dt} - \frac{di}{dt} = 0 \quad (16)$$

Assuming that the VSC is controlled by a duty ratio signal, D within [0,1] which represents a smooth equivalent signal for u, we have:

$$\frac{di}{dt} = \frac{D \cdot v_{dc} - v}{L} \quad (17)$$

where L is the VSC inductor shown in Fig. 6. For HCC operation in the active control mode, D must be in the range of $0 < D < 1$. Therefore, using (16) and (17), this inequality can be rewritten in the following form:

$$-\frac{v}{L} < \frac{di_{ref}}{dt} < \frac{v_{dc} - v}{L} \quad (18)$$

Using the HCC inductor design method in [7], [8] and [15], L can be selected as follows:

$$L = \frac{V_{dc}}{4H \cdot f_{SW}} \quad (19)$$

where V_{dc} is the steady state value of v_{dc} and f_{SW} is the maximum switching frequency of the DC/DC VSC. Substituting (19) in (18), the active control mode condition can be determined by the following equation:

$$-4H \cdot f_{SW} \cdot \frac{v}{V_{dc}} < \frac{di_{ref}}{dt} < 4H \cdot f_{SW} \cdot \frac{v_{dc} - v}{V_{dc}} \quad (20)$$

Substituting typical design values in (20), di_{ref}/dt can satisfy the active mode control condition, set by (18), because i_{ref} calculated by (12) is a smooth signal due to much slower dynamics of v and P_{ref} in comparison to the HCC high frequency operation. As a result, the HCC of the proposed PR normally operates in active control mode. Thus, considering (13) and (14), we have $|i_{ref} - i| \le H/2$. Therefore, excluding the switching ripples of i, the large signal value of i is equal to i_{ref}. As a result, considering (12), the large signal value of the VSC instantaneous active power is equal to P_{ref}. Thus, the large signal model of the DC/DC VSC shown in Fig. 6 can be presented as illustrated in Fig. 7.

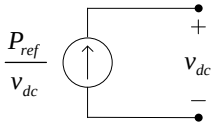

Fig. 7. Proposed large signal model for VSC PR module

C. AC/DC VSC PR

The proposed AC/DC VSC PR module is shown in Fig. 8.

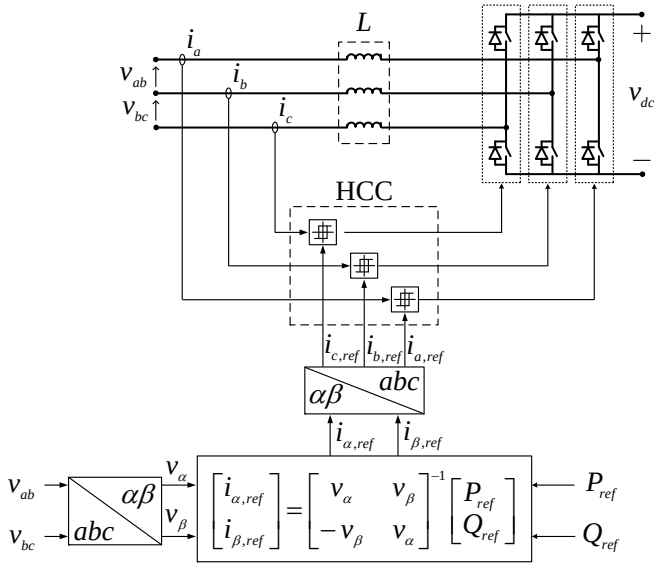

Fig. 8. AC/DC VSC PR module

As mentioned before, instantaneous power regulation with HCC is used for AC/DC VSC PR module. As shown in Fig. 8, the instantaneous power regulation is implemented by stationary reference frame variables and three two-level hysteresis regulators are used as the HCC system [7], [8]. The sliding mode analysis which was presented for the single HCC regulator of Fig. 6 can be applied to each HCC regulator of the AC/DC VSC PR. As a result, Fig. 7 can also represent the large signal model of the AC/DC VSC shown in Fig. 8.

D. VSC LVR

The interface VSC of a load has an LVR module in order to control the load supply voltage. Consequently, the active power of a load VSC is independent of the changes of its capacitive DC terminal voltage. Thus, the large signal model of a load VSC can be presented as shown in Fig. 9 where P_{Load} is the load power [15].

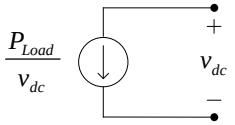

Fig. 9. Proposed large signal model for VSC LVR module

4. Proposed Large Signal Model of the DCμG

As a typical operation and control strategy for DCμG shown in Fig. 1, it is assumed that the network VSCs and the storage VSC operate as DCμG voltage regulators and the ACDG and DCDG powers are specified by their technical and economical requirements. Thus, using the developed large signal models, the large signal model of the DCμG is obtained as illustrated in Fig. 10.

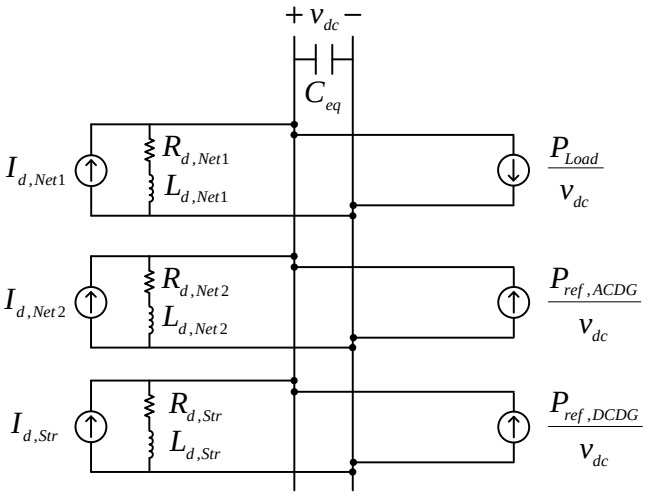

Fig. 10. Proposed large signal model of DCμG

The subindexes *Net1*, *Net2*, *Str*, *ACDG*, *DCDG* and *Load* refer to Network VSC1, Network VSC2, Storage VSC, ACDG VSC, DCDG VSC and load VSC, respectively.

Equation (10) can be rewritten for Fig. 10, as follows:

$$V_{ref,Net1} = V_{ref,Net2} = V_{ref,Str} = V_{dc,ref} \quad (21)$$

where $V_{dc,ref}$ is the DCμG reference voltage. Assuming the same values for δ_n and ω_{LP} in the DCVRs of the network and storage VSCs. C_{eq} indicates the equivalent DCμG bus capacitor which can be determined as follows:

$$C_{eq} = C_{Net1} + C_{Net2} + C_{Str} \quad (22)$$

where C_{Net1}, C_{Net2} and C_{Str} have been calculated by (9).

The proposed large signal model of DCμG provides a simple and efficient approach for studying the stability and control issues as well as the subsystem interactions in DCμGs because of its simple electrical circuit representation.

5. Modeling Verification

An effective DCμG model named control area model has been developed in [8] which can provide the same results as compared to its detailed model. Based on the concepts of the conventional Load Frequency Control (LFC) of AC power systems, the DCμG control area model has been developed considering the correspondence between AC power systems frequency and DCμG voltage behaviors. The main differences between the control area model of DCμGs and the LFC model is that the LFC model is valid for small perturbations while the DCμG control area model has been modified to include a wide range of changes [8]. Applying the control area method to the DCμG shown in Fig. 1, the following equation can be obtained:

$$\frac{V_{ref} - v_{dc,LP}}{R_{d,eq}} = C_{eq}\frac{dv_{dc}}{dt} + \frac{P_{Load} - P_{ACDG} - P_{DCDG}}{v_{dc}} \quad (29)$$

The active powers of the load and the DG units in (29) is assumed equal to their steady state values, since they are independent from DC bus voltage variations as discussed in [7].

As it can be seen, the electrical circuit equation of the large signal model in Fig. 10 is exactly the same as (29) applying (4) and (5). Thus, the proposed large signal and steady state models for the DCμG of Fig. 1 can be verified by its control area model and consequently, its detailed model.

6. Conclusion

This paper presented a novel and simple large signal model for the DCμG system including several distributed resources and loads. The proposed model has been verified by the DCμG control area model. As the control area method has been verified by the detailed DCμG model, the proposed method of this paper is valid, too. Furthermore, the proposed large signal model provides the same steady state model of DCμGs as compared to previous studies. As a result, the proposed DCμG model provides an efficient modeling approach for DCμG subsystems interacting with each other within the DCμG or within a DC power park including multiple integrated DCμGs.

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