

The design and construction of a power quality parameters recorder

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Summary

The paper presents the authors' approach to design and construction of power quality parameters recorder conforming the requirements of IEC 61000-4-30 standard. The recorder was designed and built according to the measurement algorithms developed by the authors. These algorithms meet the requirements of IEC 61000-4-30, IEC 61000-4-15 and IEC 61000-4-7 standards. Modeling of the applied algorithms and analysis of their sensitivity to variation in some parameters were carried out in a Matlab-Simulink environment. Algorithms for measuring modules were subjected to comprehensive tests verifying their correctness. Also, the tests required by relevant standards or proposed by international organizations, e.g. CIGRE [7], and additional test developed by the authors, were carried out.

Keywords: power quality, measurement, design, construction

1. Introduction

This paper presents a power quality parameters recorder designed on Matlab-dSpace platform, which is based on the international standards: IEC 61000-4-7, 61000-4-15 and 61000-4-30, that give a functional and design specification for measuring apparatus intended to indicate and assess quality of electric power supply. The paper is organized as follow. First an overview on modeling investigation is presented. Then the description of the analyzer structure is described and finally the simulation and practical tests and obtained results are discussed with conclusion.

2. Modeling investigations

The objective of the modeling investigation was to reconstruct the measuring procedure in such a manner that the relevant requirements of standardization documents were met [8-10]. The algorithms were designed to independently fulfill requirements for each parameter and provide simultaneous functioning of all other modules. The modeling investigation was carried out in Matlab-Simulink environment which ensures very good representation of mathematical models as well as good credibility and repeatability of results. Algorithms of all measuring modules were subjected to tests verifying their accuracy.

The structure of the analyzer's hardware version is presented in further sections and information on a given

measuring module structure or relevant publications, which provide its detailed description, are referred to. Consideration was also given to imprecise formulations contained in the above-mentioned standards which allow for some liberal interpretation regarding the instrument design and construction. The methods of results presentation — aggregation, smoothing, percentiles, tables, etc., were assessed, or publications describing the proposed methods proposed in standards [9,10] and other standardization documents [12,13,14], were referred to. The models of measuring modules are the basis for developing the hardware version of the power quality analyzer. Implementations were made using the rapid prototyping environment dSPACE and DS1104 board. Voltage transducers LEM CV 3-500 of very high accuracy, with 0—300 kHz bandwidth, were used as both the interface and isolating element.

The models were tested using test signals generated in the modeling environment, and the physical modules were tested using a reference instrument. The practical measurements have been performed in LV network of one university building.

3. The analyzer structure

Except of the harmonics analyzer module, where synchronous sampling was abandoned due to the hardware constraints, all modules are compliant with the developed models.

The measuring board management and readout of a part of measurement data is achieved from the ControlDesk level — an experiment management package. Code generation, programming the board and data readout are made from the Matlab level. The analyzer block diagram is shown in Fig. 1.

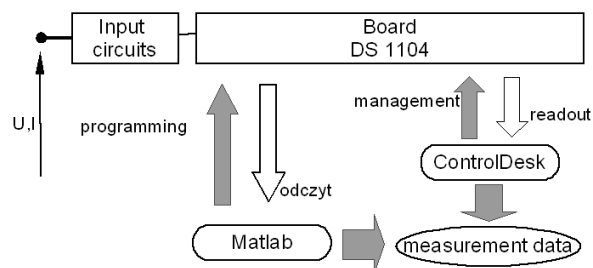


Fig. 1 Block diagram of the analyzer

Figure 1 shows both the hardware part: the input circuits of DS1104 board with analogue-digital converters and execution processor, and the concepts of programming, management and data acquisition from the board. The readout of measuring data is made from the ControlDesk

and from the Matlab level. This way of readout results from different characters of measurement data, i.e. the data obtained in specified time intervals (rms voltage value, flicker severity) and data of a random nature (voltage dips, swells).

Power quality indices can be classified into four categories in terms of the frequency of data recording:

- 200 ms aggregated values, subject to further time aggregation, e.g. rms voltage value, unbalance factor, harmonics, interharmonics,
- 10-minute short term flicker severity P_{st} values, used for evaluating the P_{lt} index,
- frequency values recorded every 10 seconds,
- parameters recorded only at the time of their occurrence — of voltage dips, swells, supply interruptions.

Recording of measurement data has been organized taking into consideration the above classification, its block diagram is shown in Fig. 2.

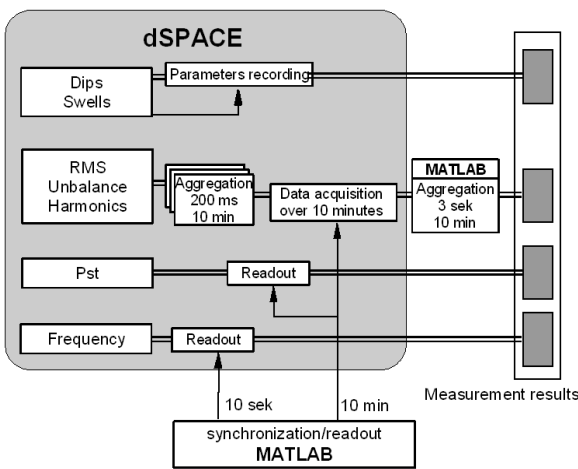


Fig. 2 Block diagram of readout and recording of the measured values

The measurement results must be timestamped with clock time whose uncertainty shall not exceed ± 20 ms (the requirement of standard [10]). As the measurement board does not support timestamping the acquired data with clock time, measurement data acquisition is performed from the level of an external application, in this case — MATLAB. In the Matlab environment a system clock of PC computer is used to timestamping the measurement results. Considering the low accuracy of PC clocks in Windows environment, the system time is synchronized with a reference clock. The synchronization is made in two ways: (i) via the Internet, using the Network Time Protocol (NTP); (ii) by means of GPS receiver. This solution may be used where Internet is inaccessible. This solution has not been applied.

In the first step the results of measurement of rms voltage value, unbalance factor, harmonic and interharmonic levels are aggregated in 200 ms time interval. The aggregation result is refreshed every ca. 1 ms; depending on the sampling frequency (10 kHz or 10240 Hz) it may give 1 ms or 0.97 ms. The data acquisition block is time-triggered from Matlab every 10 minutes because the acquisition triggering is synchronized with the clock time. The "acquisition" block reads data packets from the "200 ms aggregation" block and stores them. A subsequent triggering ends the acquisition of the

preceding 10-minute block of results, which is written to file, so the single file contains 200 ms aggregated values. Further time aggregation, i.e. 3-second, 10-minute, 2-hour, of these results is run outside the dSpace environment. Where only 10-minute aggregated values have significance for the user, the possibility of aggregation in the dSpace environment has been foreseen. The synchronized readout every 10 minutes is executed from the Matlab environment.

The short term flicker severity P_{st} is evaluated in the dSpace environment. The current value of P_{st} is computed every 20 ms. The record of P_{st} value every 10 minutes is synchronized from Matlab. The long term flicker severity P_{lt} is computed from 12 successive P_{st} values outside the dSpace environment.

Recording of the occurrence of a voltage dip/swell and its parameters is internally triggered in the dSpace environment. Each event generates a file in which parameters of this event are recorded. In the dSpace environment the time of start and end of a voltage dip/swell is recorded in the environment's relative time counted from the start of application. In order to "locate" the event on the clock time axis, the clock time of recording the file to disk is used.

The frequency value is recorded every 10 seconds; record triggering and time synchronization with the clock time is executed by Matlab.

4. Voltage rms value

A possibility of determining the rms voltage value on the basis on its definition and with the use of a low-pass FIR filter, operated in the 5–100 Hz band with Kaiser smoothing window, was taken into consideration during developing the model, whose construction specifics are given in [10]. Research has shown that the use of the filter has no negative influence on the measurement result — Fig. 3, but in the same time significantly reduces the number of arithmetical calculation. It should, however, be noted that the presented results apply to the 5–100 Hz filter. The filter used for measuring rms voltage value in a wider band, up to 2 kHz, is of much larger complexity, whereas the accuracy of measurement is lower. Therefore, for practical reasons, the rms voltage value is determined from definition.

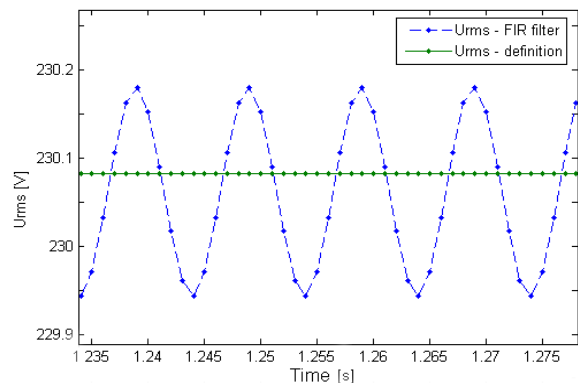


Fig. 3. The rms voltage value calculated from definition and evaluated by means of FIR filter

The full-cycle rms voltage value is calculated with the sampling frequency whereas its value in the basic 10-cycle measurement window is calculated according to rel. (1).

$$U_{rms,0.2} = \sqrt{\frac{\sum_{i=1}^N u_{rms}^2(i)}{N}} \quad (1)$$

where:

$u_{rms(i)}$ — i -th instantaneous sample of rms voltage value

N — number of rms voltage samples aggregated in time interval 200ms. The number of samples N depends on the sampling frequency.

The measurement accuracy and linearity of the rms voltage measuring module was experimentally verified over the range from 2.3 to 300 Vrms. The maximum error did not exceed 0.03 % — see table 1.

Table 1 Accuracy of the voltage rms value measurement

dSpace	Topas	Error [%]
2.31	2.31	0.001
4.63	4.61	0.007
11.48	11.47	0.001
22.96	22.94	0.007
57.48	57.46	0.007
114.94	114.92	0.007
172.42	172.4	0.007
229.91	229.91	0
249.87	249.86	0.003
287.41	287.41	0.023
299.92	299.99	0.023

The example of one-week voltage variation recorded by the developed recorder and the reference instrument Topas is presented in Fig. 4, Fig. 5 shows histogram of voltage differences in phase voltages.

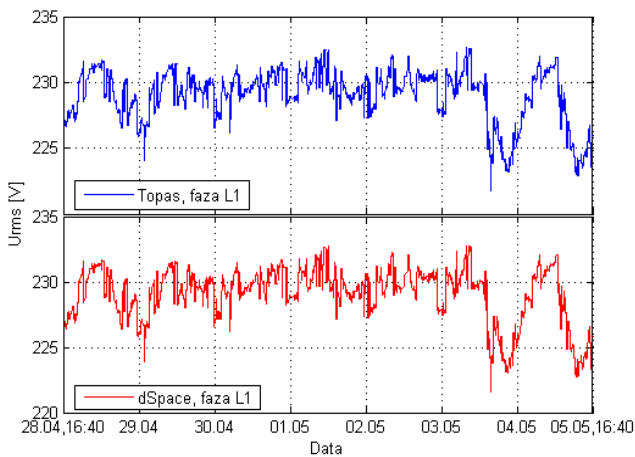


Fig. 4 An example daily graph of rms voltage value

Table 2 summarizes statistical parameters, based on 10-minute aggregated values, characterizing the voltage value in phase L1 determined using both analyzers.

Table 2 Statistical parameters of the voltage rms measurement

	Topas	dSpace	Error
Min	221.81	221.62	0.063
Mean	229.73	229.87	0.047
Max	234.36	234.35	0.003
CP05	225.55	225.55	0
CP50	230.02	230.19	0.057
CP95	232.59	232.71	0.04
CP99	233.45	233.46	0.003

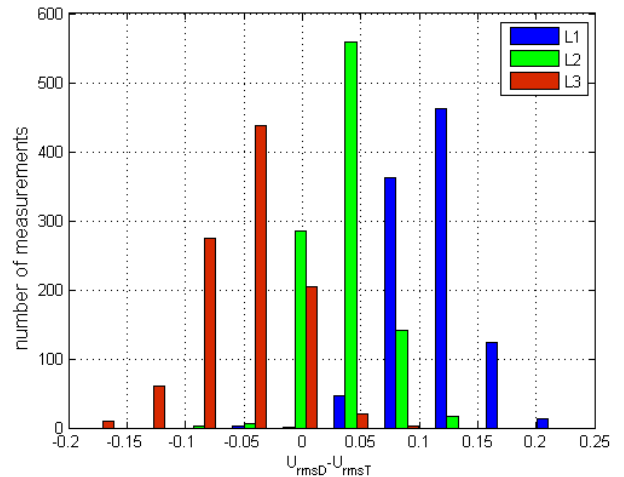


Fig. 5 Histogram of voltage differences in phase voltages.

The obtained results demonstrate very high accuracy of the rms voltage measurement. The distribution of differences (Fig. 5) confirms the random nature of errors.

5. Voltage unbalance

Usually, as a measure of voltage unbalance is taken coefficient K expressed by the ratio of negative sequence component or/and zero sequence component to the voltage or current fundamental component. In practical application is much easier to determine the voltage unbalance factor from rms voltages. Standard [10] provides relation (2) for evaluating the unbalance factor using 10-cycle rms line-to-neutral voltages.

$$K_{2U} = \sqrt{\frac{1 - \sqrt{3 - 6\beta}}{1 + \sqrt{3 - 6\beta}}} \cdot 100\% \quad (2)$$

$$\beta = \frac{U_{AB}^4 + U_{BC}^4 + U_{CA}^4}{(U_{AB}^2 + U_{BC}^2 + U_{CA}^2)^2}$$

The developed model employs also an alternative method, proposed in [15], which consists in determining the unbalance factor using the maximum deviation from the mean value of rms line-to-line voltage values (3). Averaging period is 200 ms.

$$K_{2U} = \frac{\Delta U_{\max}(U_{AB}, U_{BC}, U_{CA})}{U_{sr}} \cdot 100\% \quad (3)$$

where:

- $U_{\max}(U_{AB}, U_{BC}, U_{CA})$ — maximum deviation of any of the three line-to-line voltages from the mean value,
- U_{sr} — the mean value of three line-to-line voltages,

Table 3 shows the voltage unbalance factor values calculated according to the above three relations. The investigation was carried out for several sets of voltages. Both the voltage magnitude and phase displacements between the voltages were varied.

Table 3 The voltage unbalance factor values for different measurement methods

	U_B [Urms] [deg]	U_B [Urms] [deg]	U_C [Urms] [deg]	K_{2U} def.	K_{2U} rel. (2)	K_{2U} rel. (3)
1	167.9∠0°	184∠-120°	200.1∠120°	5.05	5.05	4.403
2	349.6∠0°	322∠-120°	294.4∠120°	4.949	4.95	4.312
3	232∠0°	240∠-121°	242∠119°	1.306	1.31	1.26
4	230∠0°	230∠-119°	230∠121°	0.582	0.58	0.505
5	230∠0°	231∠-120°	229∠120°	0.251	0.25	0.217
6	230∠0°	230∠-115°	230∠125°	2.91	2.91	2.55

Taking the values evaluated according to the unbalance factor definition as a reference, the values calculated from the relation (1) given in standard [10] are practically the same. The relation (1) is analytically identical with the definition thus the observed errors are numerical ones. The unbalance factor values computed from relation (2) contain an error of ca. 13%. the exception is No.3 set of voltages, where error is 3.5%. Considering the above results, the relation (1), proposed in standard [10], is employed for hardware implementation. It ensures a very high level of accuracy of the voltage unbalance factor representation, provided the accuracy of evaluation of rms line-to-line voltages is satisfactory.

Figure 6 shows daily variation of the unbalance coefficient measured by means of both the Topas instrument and dSpice, table 4 summarizes statistical parameters over a one week period.

Table 4 Statistical parameters of the voltage unbalance measurement

	Topas	dSpace	Error
Min	1.28	1.37	6.96
Mean	1.62	1.72	6.11
Max	1.88	2.02	7.43
CP05	1.46	1.61	8.41
CP50	1.63	1.71	4.95
CP95	1.72	1.83	6.81
CP99	1.78	1.93	8.67

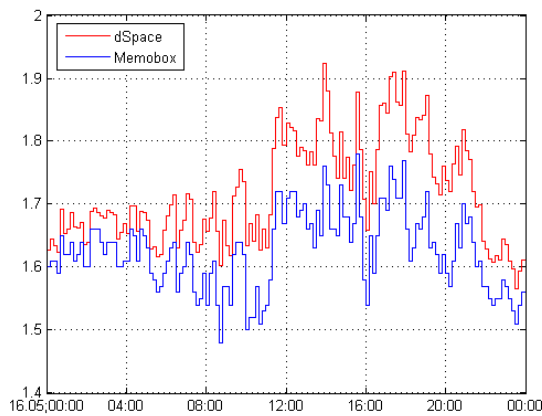


Fig. 6 Example of daily variation of the unbalance coefficient

6. Voltage distortion

The harmonics analysis module, was developed according to the requirements of standards [9] and [10], its block diagram is shown in Figure 7. Spectral analysis employs the fast Fourier transform (FFT)

technique. The model was subjected to a number of tests which confirmed its correct operation and good accuracy of analysis under conditions of heavily distorted input signal, as well as fundamental component frequency fluctuations. Testing and assessment of grouping and smoothing were also carried out, as proposed in standard [9]. The details of the model construction, performed tests and detailed analyses are presented in [16].

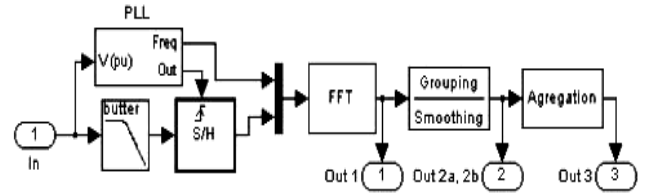


Fig. 7 Block diagram of the harmonics analysis module

Taking into account the requirements regarding synchronous sampling and considering a number of construction options, the following parameters were selected:

- sampling frequency: $f_a = 10 \text{ kHz}$,
- number of samples in the measuring window: $N = 2000$,
- measuring window width: $T_m = 0,2 \text{ sek}$.

It should be emphasized that sampling frequency of the analysis block (and therefore of all other blocks) was selected because of the necessity for rms voltage measurement to be updated every 10 ms ($U_{\text{rms}1/2}$). This time-interval governs the detection of events, i.e. voltage dips, swells and supply interruptions. The selection of 10 kHz sampling frequency, while at the same time standard [9] requires the 0.2 sec measuring window, precludes the use of radix-2 algorithms, which would significantly accelerate the execution of FFT analysis. Alteration of sampling frequency gives the number of samples 10240, ensuring 2^n samples in the measurement window as required for the radix-2 algorithms, results in evaluation of $U_{\text{rms}1/2}$ value every ca. 9.7 ms instead of 10 ms.

It has been found that the use of smoothing window, e.g. the Hanning window recommended in standard [9], reduces the spectrum blur but does not eliminate it, hence the synchronous sampling was needed. From several synchronization options, the PLL synchronization was chosen. This method has several advantages, like selectivity (capability of synchronization to the fundamental component or its multiple, also in the presence of heavy distortion) and robustness against disturbances and variation in the input signal amplitude. It, of course, is not free from disadvantages — some constructional difficulties and variability of the output signal, even in the input steady state conditions. The block diagram of the applied phase-locked loop is shown in Fig. 8.

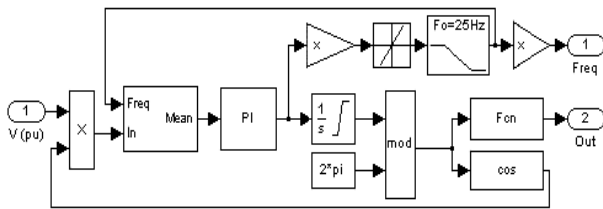


Fig. 8 The phase-locked loop (PLL) block diagram

Figure 9 shows the daily graph of THD, table 5 summarizes statistical parameters of THD measurement.

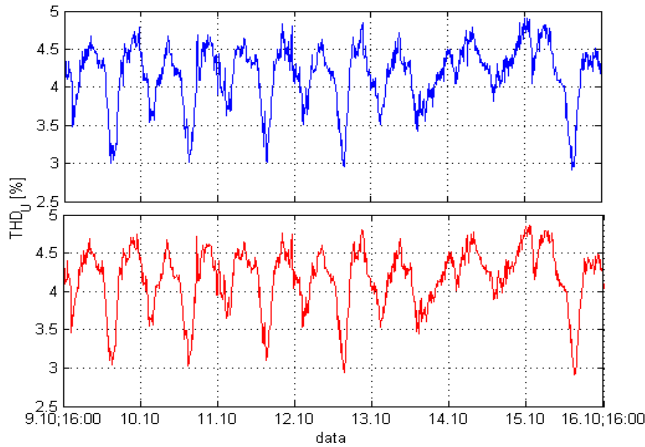


Fig. 9 One-week variation of THD

Table 5 Statistical parameters of THD measurement

	Topas	dSpace	Error
Min	2.909	2.906	0.003
Mean	4.172	4.172	0
Max	4.907	4.857	0.05
CP05	3.33	3.333	0.003
CP50	4.25	4.257	0.006
CP95	4.689	4.673	0.016
CP99	4.812	4.795	0.017

7. Flickermeter

The model has been developed according to recommendations of standard IEC 61000-4-15, which specifies the principles of flickermeter structure, provides its block diagram and specification for each block. The block diagram of the described model is shown in Figure 10.

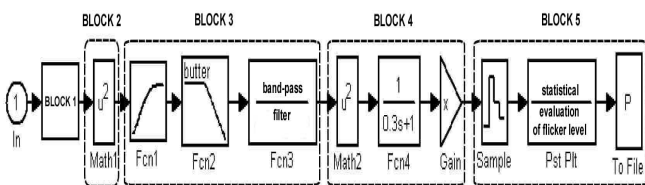


Fig. 10. Block diagram of the described flickermeter model

The detailed description of the model construction and testing is contained in publications [2,3,4,5]. Analysis of the model sensitivity to changes of selected filter parameters has been performed. Such investigation enables to check the model overall reaction to changes in parameters of a chosen filter. It enables to realize how stringent are the requirements of standard [8] concerning filter parameters. Each time the parameter of only filter

has been changed and the test 1, i.e. checking the response to square-wave signal modulation, according to the table 1 of the standard [8] was performed. Figures 11 to 13 show the test results of alterations in filter parameters for: 0.05 Hz high-pass filter, 35 Hz low-pass filter and sliding mean filter with 300 ms time constant.

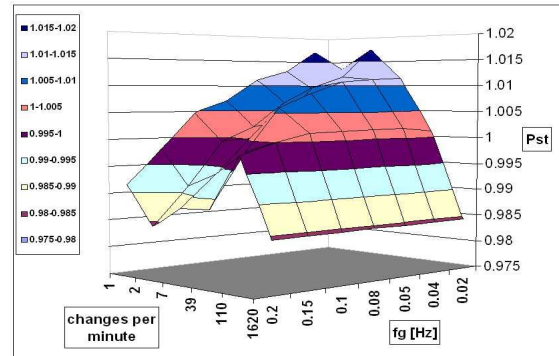


Fig. 11. Sensitivity of the model readings to the change in the high-pass filter cut-off frequency 0.05Hz [fig.10]

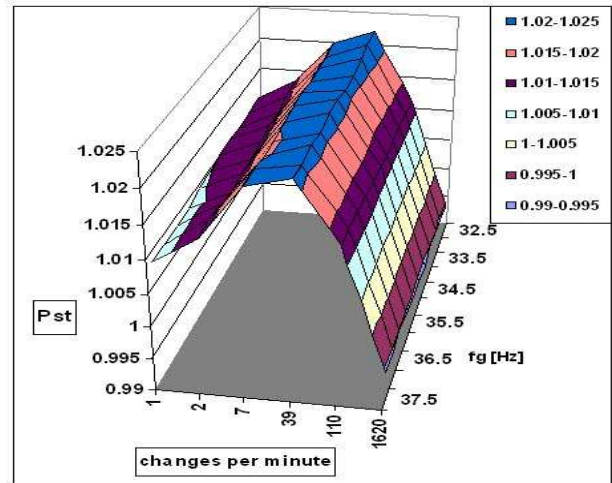


Fig. 12. Sensitivity of the model readings to the change in the low-pass filter cut-off frequency 35Hz [fig.10]

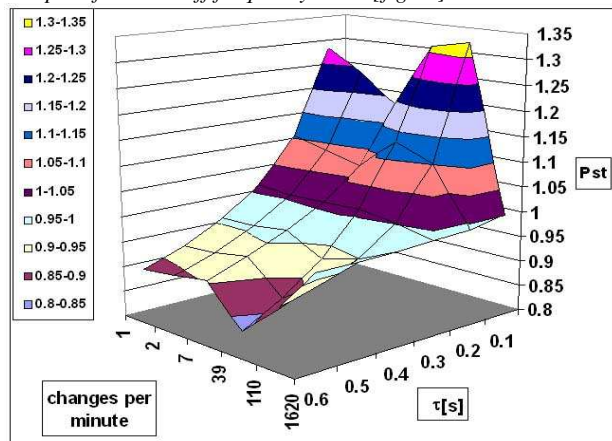


Fig. 13 Sensitivity of the model readings to change in the time constant 300ms, of the sliding mean filter [fig.10]

As can be seen from the presented results, the flickermeter developed model is not susceptible to alteration of the 0.05 Hz high-pass filter and 35 Hz low-

pass filter parameters. it is, however, highly sensitive to changes in the 300 ms sliding mean filter parameters. Within the range the time constant variation from 100 to 600 ms. The model has met the accuracy requirements only for the filter with 300 ms time constant.

Considering the test for flickermeter response to the input voltage phase jump, proposed by the CCU2/UIE Working Group on Power Quality [7], a detailed modeling investigation, described in [5], were carried out. The investigation has confirmed the flickermeter's sensitivity to this type of disturbance. The results were experimentally confirmed using the Topas recorder. The response of both the flickermeter model and Topas recorder to a constant phase jump in the measured voltage (-35°) vs. the angle at which the disturbance occurs, is shown in Figure 14.

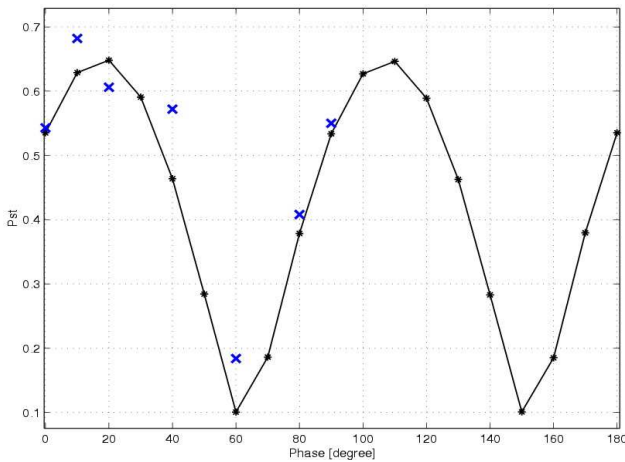


Fig. 14 Change in P_{st} as a function of the angle at which the disturbance occurred (phase jump: -35°); \times - the experiment [5]

The measuring module, developed on the basis of the flickermeter model, was subjected to test required by standard [8]. For given input signal parameters the result should be $1 \pm 5\%$. The signal parameters and results are listed in table 6.

Table 6 The results of test 1 for voltage fluctuations measurement (according to the table 5 in [8])

Number of changes per minute	Voltage change dV/V [%]	Pst
1	2.72	0.995
2	2.21	1.011
7	1.46	1.02
39	0.905	0.993
110	0.725	1.017
1620	0.402	1.027

Additionally, several control test developed on the basis of publication [1], were carried out. The results of tests 2 and 3, i.e. linearity test for square-wave and sine-wave modulation, are listed in tables 7 and 8.

Table 7 Changes in the modulating voltage and P_{st} values measured in the linearity test for square-wave modulation [1]

Test [1]	Value of k	Pst	Pst/k
2A	1	1.017	1.017
2A	10	9.658	0.965
2A	20	19.713	0.985
2B	0.2	0.217	1.085
2B	1	1.027	1.027
2B	2	2.19	1.095
2B	5	5.35	1.07
2B	10	10.74	1.074
2B	20	21.44	1.072

Table 8 Changes in the modulating voltage and Pst values measured in the linearity test for sine-wave modulation

Test [1]	Value of k	Pst	Pst/k
3A	1	1.004	1.004
3A	10	10.007	1
3A	20	19.81	0.99
3B	0.2	0.237	1.18
3B	1	1.013	1.013
3B	2	1.983	0.99
3B	5	5.003	1
3B	10	9.97	0.997
3B	20	19.997	0.99

Figure 15 shows a one-week variation of short term flicker severity, statistical parameters which characterize the voltage fluctuations measurement are tabulated in table 9.

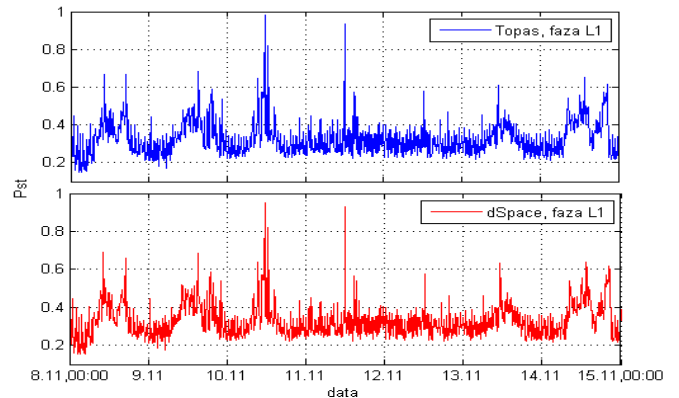


Fig. 15 The P_{st} value measured over one week

Table 9 Statistical parameters of the voltage fluctuations measurement

	Topas	dSpace	Error
Min	0.15	0.149	0.006
Mean	0.326	0.328	0.012
Max	0.984	0.953	0.158
CP05	0.224	0.228	0.02
CP50	0.309	0.313	0.02
CP95	0.488	0.492	0.022
CP99	0.605	0.613	0.043

8. Voltage dips and swells, short supply interruptions — power quality events

The model of determining power quality events was developed according to the requirements of standard [10]. The model and analysis of methods for evaluation of

these disturbances, proposed in [10] and other documents [12-14], are extensively described in [6].

9. Frequency

Considering the requirements of standard [10] related to frequency measuring, i.e. the measurement over 10-second time interval, a classical method of clock pulses counting over the cycle (or half-cycle) of the measured signal [17] was adopted. This is the one of the simplest methods for frequency measuring and allows for good accuracy over long measurement time. The accuracy depends on several factors, namely:

- The clock frequency and accuracy. i.e. on the number of samples in the measurement interval; the higher the reference clocking frequency the more accurate the measurement is. The accuracy can be improved by counting clock pulses over a larger number of cycles/half cycles.
- The accuracy of zero crossing detection.

Accuracy of zero crossing detection depends on both the sampling frequency and the level of distortion of the measured signal. In order to eliminate multiple zero-crossing the input signal should not contain harmonic and/or interharmonic components. The block diagram of the frequency measuring module is shown in figure 16.

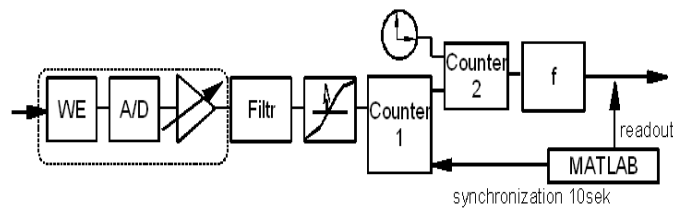


Fig. 16 Block diagram of the frequency measuring module

The frequency measuring module consists of the following function blocks:

- band-pass filter with 30-70 Hz bandwidth, which filters the harmonic and most of interharmonic components in order to eliminate multiple zero-crossing, see Fig. 17,
- zero-crossing detector,
- counter which counts the fundamental component cycles up to 499, i.e. in ca. 10 seconds interval,
- counter which counts clock pulses for 499 cycles of the fundamental component,
- frequency computing block,
- the output results latch block.

It should be noted that clock pulses are counted over the interval equal to 499 cycles of the fundamental component, what makes ca. 9.98 seconds. The shortened time of measurement enables synchronization with clock time in 10-second intervals, as required by standard [10]. According to standard [10] the results of frequency measurement do not subject to time-aggregation, nevertheless the 10-minute aggregation is maintained for the purpose of assessment.

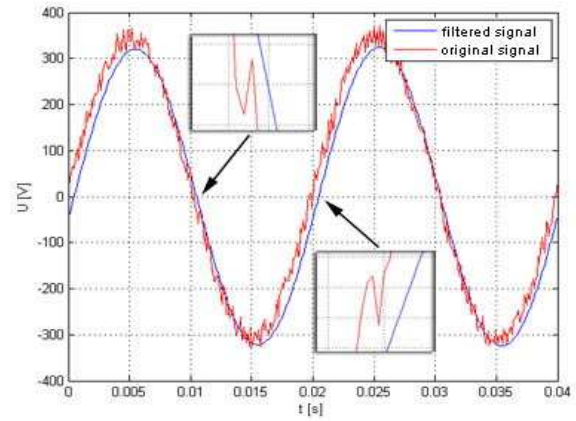


Fig. 17 Signal filtering to eliminate multiple zero-crossing

Figure 18 shows one-week recording of frequency, its statistical parameters are tabulated in table 9.

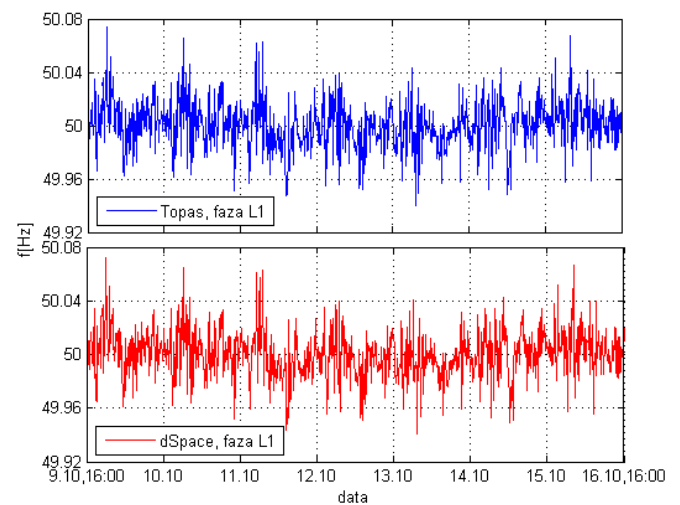


Fig. 18 The frequency value recorded over one-week measuring period

Table 10 The statistical parameters of frequency measurement

	Topas	dSpace	Error
Min	49.94	49.941	0.001
Mean	50.001	50	0.001
Max	50.074	50.072	0.003
CP05	49.973	49.972	0.002
CP50	50.001	50.001	0.001
CP95	50.03	50.029	0.001
CP99	50.043	50.042	0.001

10. Conclusions

In the authors' opinion, the information contained in standards [8-10] can be a guide for the design of power quality analyzer. These standards, however, allow for some liberal interpretation of their provisions what may lead to measurement methods based on different principles.

The developed measurement algorithms were successfully implemented in the hardware version, creating this way the power quality analyzer. Except of one limitation (the lack of synchronous sampling), the analyzer complies with the requirements of standards [8-10]. laboratory test and then experimental investigation

confirmed its measurement method is correct and accurate.

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