Study on Split-Capacitors Applied in Positive Output Super-Lift Luo-Converters

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Abstract — Voltage Lift Technique has been successfully employed in design of DC/DC converters, e.g. three series Luo-Converters. However, the output voltage increases in arithmetic progression. Super Lift Technique is the most significant contribution in Power Electronics, e.g. four series Super-Lift Converters. Their output voltage increases in geometric progression. This paper introduces a novel approach — Super Lift Technique Armed by Split-Capacitors that implements the output voltage increasing in higher geometric progression. It effectively enhances the voltage transfer gain in power series as well.

Index Terms — Voltage Lift Technique, Super-Lift Technique Armed by Split-Capacitors, Power Series, Voltage Transfer Gain.

I. INTRODUCTION

Voltage Lift (VL) Technique is a popular method widely used in electronic circuit design. It has been successfully employed in DC/DC converter applications in recent decades, and opened a way to design high voltage gain converters. Three series Luo-Converters [1–3] are the examples of VL technique implementations. However, the output voltage increases in stage by stage just along the arithmetic progression [4]. Super Lift (SL) Technique is the most significant contribution in Power Electronics, e.g. four series Super-Lift Converters [4, 5]. Their output voltage increases in geometric progression. This paper introduces a novel approach — Super Lift Technique Armed by Split-Capacitors that implements the output voltage increasing in stage by stage along higher geometric progression. It effectively enhances the voltage transfer gain in power series as well [6 - 8].

Assume no power losses during the conversion process, \( V_{in} \times I_{in} = V_{O} \times I_{O} \). The voltage transfer gain is \( G = \frac{V_{O}}{V_{in}} \).

II. SPLIT-CAPACITORS

A capacitor \( C_1 \) as shown in Figure 1 (a) can be split into two parts: two capacitors \( C_1 \) and \( C_2 \) as shown in Figure 1 (b); and three parts: three capacitors \( C_1 \), \( C_2 \) and \( C_3 \) as shown in Figure 1 (c). Furthermore, it can be split into \( \alpha \) parts that are shown in Figure 1 (d).

The split stage can be defined \( \alpha \)-times. Now, we define the single capacitor to be in \( \alpha = 1 \) split stage as shown in Figure 1 (a); We define the two split capacitors to be in \( \alpha = 2 \) split stage as shown in Figure 1 (b), the slave switch \( S \) is exclusively switched with the Main switch \( S \); We define the three split capacitors to be in \( \alpha = 3 \) split stage as shown in Figure 1 (c), the slave switches \( S \) and \( S \) are exclusively switched with the Main switch \( S \). We define the \( \alpha \) split capacitors to be symbolized by \( \alpha C \). These capacitors can be charged by a DC voltage \( V_{in} \). In the steady-state, each capacitor is assumed to be charged to the source voltage \( V_{in} \). All split capacitors are charged by source voltage \( V_{in} \) in parallel. When the capacitors are discharged, all split capacitors are discharged by an external voltage in series.

III. SPLIT CAPACITORS APPLIED IN THE ELEMENTARY POSITIVE OUTPUT SUPER-LIFT LUO-CONVERTER

Elementary positive output (P/O) super-lift Luo-converter is shown in Figure 2. Its circuit diagram in Figure 2 (a), and its equivalent circuits in switch-on and switch-off are shown in Figure 2 (b) and (c) respectively.
Figure 2. Elementary P/O SL Luo-Converter: (a) Circuit diagram, (b) Equivalent circuit during switching-on, (c) Equivalent circuit during switching-off.

The Elementary circuit and its equivalent circuits during switching-on and -off are shown in Figure 2. The voltage across capacitor C1 is charged to \( V_{in} \) in the steady state. The current \( i_L \) flowing through inductor L increases with voltage \( V_{in} \) during switching-on period \( kT \) and decreases with voltage \(-V_{O} - 2V_{in}\) during switching-off period \((1 - k)T\). Therefore, the ripple of the inductor current \( i_L \) is:

\[
\Delta i_L = \frac{V_{in} kT}{L} = \frac{V_{O} - 2V_{in}}{L} (1-k)T
\]

The voltage transfer gain is

\[
G = \frac{V_{O}}{V_{in}} = \frac{2-k}{1-k}
\]

A. A 2 Split Capacitors (\( \alpha = 2 \)) Applied in The Elementary P/O SL Circuit.

If the capacitor \( C_1 \) is split to two capacitors \( C_1 \) and \( C_2 \). The circuit and its equivalent circuits during switching-on and -off are shown in Figure 3 (as mentioned that the slave switch S1 is exclusive switch with the Main switch S).

Figure 3. A two split capacitors applied in the Elementary P/O SL Luo-Converter: (a) Circuit diagram, (b) Equivalent circuit during switching-on, (c) during switching-off.

The voltage across capacitors \( C_1 \) and \( C_2 \) are charged to \( V_{in} \) in the steady state. The current \( i_L \) flowing through inductor L increases with voltage \( V_{in} \) during switching-on period \( kT \) and decreases with voltage \(-V_{O} - 4V_{in}\) during switching-off period \((1 - k)T\). Therefore, the ripple of the inductor current \( i_L \) is:

\[
\Delta i_L = \frac{V_{in} kT}{L} = \frac{V_{O} - 4V_{in}}{L} (1-k)T
\]

The voltage transfer gain is

\[
G = \frac{V_{O}}{V_{in}} = \frac{4-3k}{1-k}
\]

B. A 3 Split Capacitors (\( \alpha = 3 \)) Applied in The Elementary P/O SL Circuit.

If the capacitor \( C_1 \) is split to three capacitors \( C_1, C_2 \) and \( C_3 \). The circuit and its equivalent circuits during switching-on and -off are shown in Figure 4 (as mentioned that the slave switches S1 and S2 are exclusively switched with the Main switch S).

Figure 4. Elementary P/O SL Luo-Converter armed by three split capacitors. (a) Circuit diagram; (b) Equivalent circuit during switching-on; (c) during switching-off.

The voltage across capacitors \( C_1, C_2 \) and \( C_3 \) are charged to \( V_{in} \) in the steady state. The current \( i_L \) flowing through inductor L increases with voltage \( V_{in} \) during switching-on period \( kT \) and decreases with voltage \(-V_{O} - 3V_{in}\) during switching-off period \((1 - k)T\). Therefore, the ripple of the inductor current \( i_L \) is:

\[
\Delta i_L = \frac{V_{in} kT}{L} = \frac{V_{O} - 3V_{in}}{L} (1-k)T
\]

The voltage transfer gain is

\[
G = \frac{V_{O}}{V_{in}} = \frac{3-2k}{1-k}
\]

C. A \( \alpha \) Split Capacitors Applied in the Elementary P/O SL Circuit.

If the capacitor \( C_1 \) is split to \( \alpha \) capacitors, the circuit is shown in Figure 5.

Figure 5. A \( \alpha \) split capacitors applied in the Elementary P/O SL Luo-Converter.
The voltage across the α capacitors are charged to $V_{in}$ in parallel during switch-on in the steady state. The current $i_L$ flowing through inductor $L$ increases with voltage $V_{in}$ during switching-on period $kT$ and decreases with voltage $-V_O - (\alpha + 1)V_{in}$ during switching-off period $(1 - k)T$. Therefore, the ripple of the inductor current $i_L$ is:

$$\Delta i_L = \frac{V_{in}}{L} kT = \frac{V_O - (\alpha + 1)V_{in}}{L} (1 - k)T$$  \hspace{1cm} (7)

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \frac{\alpha + 1 - \alpha k}{1 - k}$$  \hspace{1cm} (8)

**IV. MAIN SERIES**

The Main series has several Circuits such as Re-lift circuit, Triple-lift circuit and high-order-lift circuit. We defined the stage as $n = 1$ means Elementary circuit; $n = 2$ means Re-Lift circuit, $n = 3$ means Triple-lift circuit, and $n$ can be higher number means the high-order-lift circuit. Figure 5 shows the Elementary circuit. Figure 6 shows the Re-Lift circuit, and Figure 7 shows the Triple-Lift circuit.

**Figure 6. The Re-Lift circuit**

The voltage transfer gain of the Re-Lift circuit is

$$G = \frac{V_O}{V_{in}} = \left(\frac{\alpha + 1 - \alpha k}{1 - k}\right)^n$$  \hspace{1cm} (9)

The voltage transfer gain of the Triple-Lift circuit is

$$G = \frac{V_O}{V_{in}} = \left(\frac{\alpha + 1 - \alpha k}{1 - k}\right)^3$$  \hspace{1cm} (10)

The voltage transfer gain of the nth-order-Lift circuit, if each stage use split capacitor $\alpha C$, the voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \left(\frac{\alpha + 1 - \alpha k}{1 - k}\right)^n$$  \hspace{1cm} (11)

It is a very high voltage transfer gain. For example, if $V_{in} = 20 V$, $n = 3$, $\alpha = 4$ and $k = 0.5$, the voltage transfer gain $G$ is equal to 216. The output voltage will be 4320 V!

**V. MEC, SPLIT CAPACITORS USED IN DEC**

The original Double/Enhance Circuit (DEC) is shown in Figure 8, which consist of two diodes ($D_{11}$ and $D_{12}$) and two capacitor ($C_{11}$ and $C_{12}$).

**Figure 8. The Double/Enhanced Circuit (DEC)**

The output voltage is

$$V_O = 2V_{in}$$  \hspace{1cm} (12)

If the capacitor $C_{11}$ replaced by a $\gamma$-split Capacitor $\gamma C$ as show in Figure 9. We can call it Multiple/Enhance Circuit (MEC).

**Figure 9. Multiple/Enhance Circuit (MEC)**

The output voltage will be

$$V_O = (\gamma + 1)V_{in}$$  \hspace{1cm} (13)

**VI. ADDITIONAL SERIES**

All circuits of Positive Output Super-Lift Converters – Additional Series are derived from the corresponding circuits of the main series. We can add a MEC following all circuits to obtain the circuits of the Additional Series.

The first three stages of this series are shown in Figures 10 – 12. For convenience to explain, we call them Elementary additional circuit, Re-Lift additional circuit and Triple-Lift additional circuit respectively. We can number them as $n = 1$, 2 and 3.

**A. Elementary additional circuit**

This circuit is derived from Elementary circuit with adding a MEC ($D_{11}$-$D_{12}$-$\gamma C$-$C_{12}$). Its circuit and switch-on and -off equivalent circuits are shown in Figure 10.

**Figure 10. Elementary additional circuit**

(a) Circuit diagram
The voltage across all capacitor $\alpha C_2$ is $V_1$ in steady state as shown in Equation (11). The inductor current increases during switch $S$ on, and decreases during switch $S$ off. The current variation is
\[
\frac{V_i}{L_2} kT = \frac{V_o - \gamma V_i - V_{\alpha 1}}{L_2} (1-k)T
\]
Therefore the output voltage $V_o$ is
\[
V_o = \left[ -\frac{1}{1-k} + \gamma \frac{\alpha + 1 - \alpha k}{1-k} \right] V_i
\]  
\[(15)\]

**B. Re-Lift additional circuit**

This circuit is derived from Elementary additional circuit by adding the parts (L$_3$-D$_6$-D$_7$-D$_8$-C$_5$-C$_6$). Its circuit diagram is shown in Figure 11.

\[\text{Figure 10. Elementary additional circuit}\]

The voltage across capacitor $C_2$ is charged to $V_1$ and voltage across capacitor $C_4$ is charged to $V_2$. All $\gamma C$ is charged to $V_2$. The $V_2$ is shown in Equation (13). The second inductor current increases during switch $S$ on, and decreases during switch $S$ off. The current variation is
\[
\frac{V_i}{L_2} kT = \frac{V_o - \gamma V_i - V_{\alpha 1}}{L_2} (1-k)T
\]
and
\[
V_2 = \frac{\alpha + 1 - \alpha k}{1-k} V_i
\]
Therefore the output voltage $V_o$ is
\[
V_o = \left[ -\frac{1}{1-k} + \gamma \frac{\alpha + 1 - \alpha k}{1-k} \right] V_i
\]  
\[(16)\]

**C. Triple-Lift additional circuit**

This circuit is derived from Re-Lift additional circuit by adding the parts (L$_3$-D$_6$-D$_7$-D$_8$-C$_5$-C$_6$). Its circuit diagram is shown in Figure 12.

\[\text{Figure 12. Triple-Lift additional circuit}\]

The voltage across capacitor $C_2$ is charged to $V_1$. The voltage across capacitor $C_4$ is charged to $V_2$ and voltage across capacitor $C_6$ is charged to $V_3$. All $\gamma C$ is charged to $V_3$ shown in Equation (15). The inductor current increases during switch $S$ on, and decreases during switch $S$ off. The current variation is
\[
\frac{V_i}{L_3} kT = \frac{V_o - \gamma V_i - V_{\alpha 1}}{L_3} (1-k)T
\]
and
\[
V_3 = \frac{\alpha + 1 - \alpha k}{1-k} V_2
\]
Therefore the output voltage $V_o$ is
\[
V_o = \left[ -\frac{1}{1-k} + \gamma \frac{\alpha + 1 - \alpha k}{1-k} \right] V_i
\]  
\[(17)\]

**D. Higher Order Lift additional circuit**

Higher Order Lift additional circuit can be designed by just multiple repeating the parts (L$_3$-D$_6$-D$_7$-D$_8$-C$_5$-C$_6$). For nth order lift additional circuit, the final output voltage is
\[
V_o = \left[ -\frac{1}{1-k} + \gamma \frac{\alpha + 1 - \alpha k}{1-k} \right] V_i
\]  
\[(18)\]

**VII. SUMMARY OF P/O SUPER-LIFT Luo-Converters APPLYING SPLIT CAPACITORS**

All circuits of Positive Output Super-Lift Luo-Converters using split capacitors $\alpha C$ and MEC (with $\gamma C$) as a family can be shown in Figure 13 (the family tree). From the analysis of previous two sections we can have the common formula to calculate the output voltage:
\[
V_o = \left[ \frac{1}{1-k} + \gamma \frac{\alpha + 1 - \alpha k}{1-k} \right] V_i
\]
\[\text{main\_series}\]
\[
\left[ \frac{1}{1-k} + \gamma \frac{\alpha + 1 - \alpha k}{1-k} \right] V_i
\]
\[\text{additional\_series}\]
\[
\left[ \frac{1}{1-k} + \gamma \frac{\alpha + 1 - \alpha k}{1-k} \right] V_i
\]
\[\text{additional\_series}\]
\[
\left[ \frac{1}{1-k} + \gamma \frac{\alpha + 1 - \alpha k}{1-k} \right] V_i
\]
\[\text{additional\_series}\]
VIII. SIMULATION RESULTS

To verify the design and calculation results, P-Sim simulation package was applied to these converters. We checked the Re-lift circuit with \( n = 2 \) and \( \alpha = 2 \). Choosing \( V_{in} = 20 \text{ V} \), \( L_1 = L_2 = 10 \text{ mH} \), all Capacitances are \( 2 \mu\text{F} \) and \( R = 30 \text{ k}\Omega \), and using \( k = 0.5 \) and \( f = 50\text{kHz} \).

A. Simulation results of a Re-lift circuit

We obtain the voltage values \( V_{in} \) and \( V_O \) of a Re-lift circuit (with \( n = 2 \) and \( \alpha = 2 \)) to be 20 V and 320 V respectively. The simulation results are shown in Figure 14. The voltage values are matching on the calculated results.

B. Simulation results of a Re-lift additional circuit

We obtain the voltage values \( V_{in} \) and \( V_O \) of a Re-lift additional circuit (with \( n = 2 \), \( \alpha = 2 \) and \( \gamma = 2 \)) to be 20 V and 800 V respectively. The simulation results are shown in Figure 15. The voltage values are matching on the calculated results.

IX. EXPERIMENTAL RESULTS

A test rig was constructed to verify the design and calculation results, and compare with P-Sim simulation results. We still choose \( V_{in} = 20 \text{ V} \), all inductances are \( 10 \text{ mH} \), all Capacitances are \( 2 \mu\text{F} \) and \( R = 30 \text{ k}\Omega \). The duty cycle is \( k = 0.5 \) and \( f = 50\text{kHz} \). The component of the switch is a MOSFET device IRF950 with the rates 1000V/5A/2MHz. We measured the values of the input and output voltages in following converters.

A. Experimental results of a Re-lift circuit

After carefully measuring a Re-lift circuit (with \( n = 2 \) and \( \alpha = 2 \)), we obtained the input voltage value of \( V_{in} = 20 \text{ V} \) (shown in Channel 1 with 5.0 V/Div) and output voltage value of \( V_O = 320 \text{ V} \) (shown in Channel 2 with 50 V/Div). The experimental results are shown in Fig. 16, which are identically matching on the calculated and simulation results, which are \( V_{in} = 20 \text{ V} \) and \( V_O = 320 \text{ V} \) shown in Fig. 14.

B. Experimental results of a Re-lift additional circuit

After carefully measuring a Re-lift additional circuit (with \( n = 2 \), \( \alpha = 2 \) and \( \gamma = 2 \)), we obtained the input voltage value of \( V_{in} = 20 \text{ V} \) (shown in Channel 1 with 5.0 V/Div) and output voltage value of \( V_O = 800 \text{ V} \) (shown in Channel 2 with 100...
The experimental results are shown in Fig. 17, which are identically matching on the calculated and simulation results, which are $V_{in} = 20$ V and $V_O = 800$ V shown in Fig. 15.

Figure 17. Experimental results of a Re-lift additional circuit

X. ACKNOWLEDGEMENT

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XI. CONCLUSION

A new method to enhance the voltage transfer gain of DC/DC converters – Split Capacitors applied in Positive Output Super-Lift Luo-Converters has been successfully created. It largely increases the voltage transfer gain in power series. Very high output voltage is easily obtained. Simulation and experimental results verified the design and calculations. This series Luo-Converters will be applied in industrial applications with very high output voltage.

REFERENCES


Biographies

Dr. Fang Lin Luo (IEEE M’84 – SM’95) received his Bachelor Sc. Degree, First Class with Honours in Radio-Electronic Physics from the Sichuan University, Chengdu, Sichuan, China and his Ph. D. Degree in Electrical Engineering and Computer Science (EE & CS) from Cambridge University, England, UK in 1986. He is with the School of Electrical and Electronic Engineering, Nanyang Technological University (NTU), Nanyang Avenue, Singapore 639798, and also with the AnHui University of Technology, AnHui 243002, China.

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Dr. Luo was the Chief Editor of the International journal <Power Supply Technologies and Applications> in 1998-2003. He is the International Editor of the International journal <Advanced Technology of Electrical Engineering and Energy>. He is currently the Associate Editor of the IEEE Transactions on both Power Electronics and Industrial Electronics. Dr. Luo was the General Chairman of the IEEE conference ICIEA’2006, 24-26 May 2006 in Singapore, and is the General Chairman of the ICIEA’2008, 3-5 June 2008 in Singapore.

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