3-Phase Line-Interactive Dynamic Voltage Restorer with Hybrid Sag Detection Algorithm

Byung M. Han, Jong-Kyu Jeong, and Ji-Heon Lee
Department of Electrical Engineering
Myongji University
San 38-2 Namdong Yongin, Gyeonggi-do (South Korea)
Phone/Fax number:+82-31-330-6366, e-mail: erichan@mju.ac.kr

Abstract. This paper describes the development of a 3-phase line-interactive DVR with a hybrid sag detection algorithm. The developed detection algorithm has a hybrid structure composed of an instantaneous detector and the RMS-variation detectors. The source voltage passes through the sliding-window DFT and RMS calculator, and the instantaneous sag detection part. If instantaneous sag is detected, the RMS variation detector-1 is selected to calculate the RMS variation. The RMS variation detector-2 is selected when the instantaneous sag occurs under the operation of the RMS variation detector-1. The feasibility of proposed algorithm was verified through computer simulations and experimental works with reference to a prototype of line-interactive DVR with 3kVA rating. The line-interactive DVR with proposed algorithm can compensate the input voltage sag and interruption within 2ms delay. The developed DVR can effectively compensate the voltage sag or interruption for the sensitive load, such as computer, communication equipment, and automation equipment.

Key words
Line-Interactive, DVR (Dynamic Voltage Restorer), Phase-Locked Loop, RMS variation detector, DFT (Discrete Fourier Transform).

1. Introduction

Recently computer, communication devices, automation devices come into wide use in the office, industry, and even home. These devices, which operate continuously during 24 hours, require highly reliable input power. Supplying unreliable input power to these devices brings about severe loss to the customer. One of the input power disturbances is the voltage sag or interruption due to the fault in the interconnected power system [1, 2].

The compensator for voltage sag or interruption is called DVR (dynamic voltage restorer) [3]. DVR for the voltage sag does not require energy storage unit, while DVR for voltage interruption requires it. DVR is divided into two types with reference to the connection pattern. DVR connected in series with load through transformer is the most common structure [4]. One severe disadvantage of this configuration is high system loss due to the continuous operation. Another disadvantage is the delicate protection due to series connection of system.

DVR connected in parallel with load and operated with line-interactive scheme is another structure. One strong advantage is relatively low system rating and loss because DVR operates only for disturbance time. However, one disadvantage is the compensation delay between the disturbed point and the compensated point, which is critical in system performance. Another disadvantage is the conduction loss of source separation switch, which conducts the load current continuously in normal state.

Major part of the compensation delay is the detection delay for the voltage sag or interruption [5,6]. Instantaneous detection is a rapid way to detect the voltage sag or interruption, but it is not applicable for the distorted input voltage. RMS detection is an accurate way to detect the voltage interruption, but it takes quarter-period of delay time.

This paper proposes a hybrid structure of fast sag detection algorithm in a line-interactive three-phase DVR, which is composed of an instantaneous detection part and two RMS-variation detectors. Also, a new switching scheme for load separation switch is proposed to offer reliable system operation. The performance verification of proposed algorithm was carried out through computer simulations, and the hardware implementation was confirmed by experimental works with a prototype of line-interactive DVR with 3kVA rating.

2. Proposed Detection Algorithm

The waveform of one-phase voltage can be expressed by equation (1), considering the harmonic components.

\[ v(t) = \sum_{n=1}^{N} V_n \sin(n\omega t + \theta_n) \]  

(1)

If the voltage waveform is composed of only the fundamental component, the value of \( n \) is equal to 1.
Otherwise, the value of n is an integer larger than 1. In case of sinusoidal input voltage, it is easy to detect the sag or interruption fast and precisely by checking the instantaneous value.

However, the real input voltage contains harmonic components, which brings about difficulty to detect the sag or interruption. The RMS detection scheme was proposed to solve this weak point. However, this method causes a delay time in detection because it takes time to compute the RMS value from the instantaneous value.

In order to solve these weak points, this paper proposes a novel algorithm, which is composed of the instantaneous detection and the RMS variation detection using DFT method.

The measured input voltage is converted into a signal with unit magnitude, dividing it by the peak value as the following equation (2).

\[ v_{pu} = \frac{v(t)}{v_{peak}} \]  

Normally the input voltage has distortion. So, this voltage is converted into a unit sine signal passing through the PLL circuit. This unit sine signal used to generate a reference signal for instantaneous sag detection. The reference signal has 90% of the unit sine signal around the peak point, and zero value around the zero-crossing point as shown in Fig. 1.

The reference signal for instantaneous detection \( v_{sag\_ref} \) can be expressed by equation (3).

\[ v_{sag\_ref} = \begin{cases} 
0.9 \times \sin \omega_i \theta, & \theta_i \leq \theta \leq \pi - \theta_i \\
0, & -\theta_i < \theta < \theta_i 
\end{cases} \]  

Where, \( \theta_i \) is 20°, and the sine value of \( \theta_i \) is 0.3.

A distorted input voltage and the reference signal for instantaneous sag detection as shown in Fig. 1. When the voltage signal is lower than the reference, the instantaneous detection scheme recognizes it as the voltage sag, although it is actually not. So, a double checking scheme is required. In this proposed algorithm, an RMS variation of the fundamental component is measured to judge the voltage sag. And a DFT (Discrete Fourier Transform) algorithm is used to calculate the RMS value of fundamental component.

The source voltage \( v(t) \) can be expressed as the following equation (4) using the Fourier series.

\[ v(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega_T t + \sum_{n=1}^{\infty} b_n \sin n\omega_T t \]  

The fundamental component for \( n=1 \) is obtained as in equation (5) and (6), separating the real part and imaginary part.

\[ a_1 = \frac{2}{T} \int_0^T v(t) \cos \omega_T t \, dt \]  
\[ b_1 = \frac{2}{T} \int_0^T v(t) \sin \omega_T t \, dt \]  

Applying the DFT for equation (5) and (6), equation (7) and (8) are obtained.

\[ a_i = \sqrt{\frac{2}{N}} \sum_{i=0}^{N-1} v(t-i\frac{T}{N}) \cos \left( \frac{2\pi i}{N} \right) \]  
\[ b_i = \sqrt{\frac{2}{N}} \sum_{i=0}^{N-1} v(t-i\frac{T}{N}) \sin \left( \frac{2\pi i}{N} \right) \]  

Using the value of \( a_1 \) and \( b_1 \), the RMS value of fundamental component can be easily obtained as the following.

\[ V_{RMS} = \sqrt{a_1^2 + b_1^2} \]  

Fig. 2. Hybrid detection method for voltage interruption

Fig. 2 shows the structure of hybrid detection method which consists of an instantaneous detector, RMS
variation detector-1, and RMS variation detector-2. The source voltage passes through the sliding-window DFT and RMS calculations and the instantaneous sag detector. If instantaneous sag occurs while the RMS variation detector-1 is under operation, it is impossible to calculate the RMS variation within 1ms. So, the RMS variation detector can not successfully detect the sag. In order to remove this weak point, the RMS variation detector-2 starts to operate at this moment. Therefore, two state machines of RMS variation detector operate in parallel with complementary role. The critical value \( \Delta E \) is determined by the minimum RMS variation obtained at the instant when the sag occurs at \( n\pi + 20^\circ \). The proposed algorithm offers a fast detection of voltage sag, which makes the DVR compensate it within 2.0ms.

If the instantaneous sag occurs while the RMS variation detector-1 is under operation, it is impossible to calculate the RMS variation within 1ms. So, the RMS variation detector-1 cannot successfully detect the actual sag. In order to remove this weak point, the RMS variation detector-2 starts to operate at this moment. Therefore, two state machines of RMS variation detector operate in parallel with complementary role. The critical value \( \Delta E \) is determined by the minimum RMS variation obtained at the instant when the sag occurs at \( n\pi + 20^\circ \). The proposed algorithm offers a fast detection of voltage sag, which makes the DVR compensate it within 2.0ms.

Fig. 3 shows simulation results obtained from the proposed sag detection algorithm. The instantaneous sag is detected when the input voltage is lower than the reference signal as shown in the 3rd graph. Two RMS variation detectors are selected according to the operation flow shown in Fig. 2. Although the two RMS variation detectors are selected many times under the instantaneous sag situations, the calculated RMS variation is larger than the critical value. It is confirmed that there is no real sag for the first cycle. According to the 2nd graph, it is known that the detection delay is about 0.8ms.

3. Line-Interactive DVR

A. System Configuration

Fig. 4 shows the configuration of the DVR with proposed algorithm including the source and the load. The DVR consists of three full-bridge inverter to control each phase voltage, super-capacitor, power transformer, anti-parallel thyristor switches, and system controller. In normal state the source supplies power directly to the load through the thyristor switch. When the voltage interruption occurs, the controller detects the disturbance and the inverter supplies nominal voltage through the power transformer by discharging the super-capacitor, in which the anti-parallel thyristor switch turns off to separate the source.

![Fig. 4. Configuration of Proposed 3-Phase Line-Interactive DVR](image)

When the source is recovered, the compensating voltage is removed by cutting off the gate signals for the inverter. The thyristor switch turns on to supply power from the source. After elapsing a few seconds, the inverter starts charging the super-capacitor to be ready for the next disturbance.

The measured source voltage is sent to the phase-locked loop to obtain the unit sine signal, which is needed to calculate the reference value for instantaneous sag detection. DFT operation is carried out in sliding-window pattern for half-period of power frequency. The source voltage is passed through the hybrid detection flow in Fig. 2. Once the sag is detected, the inverter injects a sinusoidal voltage obtained from the current and voltage control procedures.

The DC voltage and AC current of three full-bridge inverter are sent to the DC voltage and AC current control. The load voltage and current, the source current, and the full-bridge inverter current are sent to the AC voltage control. The output of these control blocks are sent to the MUX. The output of MUX is sent to the PWM pulse generator. The unit sine from the phase-locked loop is sent to the gate pulse generator for the anti-parallel thyristor switches.

The size of super-capacitor bank is determined depending on duration of the voltage interruption and size of the connected load. It is assumed that the voltage interruption has duration of 4 seconds and the load has a power rating.
of 3kVA. Therefore, total energy to be released during the voltage interruption is designed to be 12kJ. The bank of super-capacitor is designed considering the size of energy storage, the DC link voltage, the voltage and current rating of each capacitor unit. Table I shows the specification of the selected super-capacitor.

<table>
<thead>
<tr>
<th>Items</th>
<th>Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated working voltage</td>
<td>2.7VDC</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>-40 to +60°C</td>
</tr>
<tr>
<td>Nominal Cap. Range</td>
<td>100F</td>
</tr>
<tr>
<td>Equivalent Series Resistance</td>
<td>0.014Ω(1kHz)</td>
</tr>
</tbody>
</table>

The bank is designed so as to utilize the upper 20% of maximum storage capacity, considering the expandability of operation capacity. The maximum current flows through the super-capacitor bank when it discharges the maximum power. The minimum voltage across the super-capacitor bank can be determined with the maximum discharge power and the current rating.

It is assumed that the super-capacitor is charged by 2.5V, which is 92% of the maximum charging voltage of 2.7V, considering 8% margin. The lowest discharge voltage is determined to be 2.0V. Therefore, the minimum DC link voltage and the lowest discharge voltage determine the number of super-capacitor units. 100 units of super-capacitor were connected in series for enough safety margins.

B. Thyristor Switch Operation

The line-interactive DVR with proposed algorithm has an anti-parallel thyristor switch at each phase in Fig. 5. It holds on-state in normal operation, and disconnects the source when the sag or interruption occurs.

If the inverter starts to compensate at the instant when the thyristor switch is on, the inverter current flows into the source side instead of the load side. Since the source impedance is very small, the inverter supplies overcurrent and burns down. The load voltage can not be restored. Because of this, the inverter starts to compensate after the thyristor switch turns off by compulsion.

At band 1, since both gate pulses for Th1 and Th2 are in on-state, both the source voltage and the inverter voltage are positive at the instant of sag. Even though both thyristor gate pulses are removed after detecting the sag, Th1 turns off and Th2 holds the conduction state on the contrary. This causes the reverse current flow. In order to prevent the reverse current, the system detects the load current and makes both thyristor switches turn off.

At band 2, since both gate pulses for Th1 and Th2 are in on-state, both the source voltage and the inverter voltage are negative at the instant of sag. Even though both thyristor gate pulses are removed after detecting the sag, Th2 turns off and Th1 holds the conduction state. This causes the reverse current flow. In order to prevent the reverse current, the system detects the load current and makes both thyristor switches turn off.

When the voltage sag occurs, the inverter injects a voltage after the controller turns off the thyristor switch by checking the phase angle of source voltage and that of source current. Equation (10) represents the inverter output voltage in order to turn off the thyristor switch.

\[ v_{inv} = v_{src}K_T + L\frac{I_{src}}{K_T T} \]

Where, \( L \) is the leakage inductance of transformer, \( T \) is the control operation period, \( K_T \) is the turn ratio of transformer, and \( I_{src} \) is the source current at the instant of sag.

The turn-off time of thyristor switch is determined by dividing the calculated source voltage by the minimum inverter voltage. The thyristor switch is turned off considering the voltage difference due to transformer characteristic.

C. Inverter Output Voltage Control

When the sag or interruption occurs, the full-bridge inverter supplies the load with a nominal voltage after preventing the reverse current flow. Fig. 6 shows a voltage control scheme developed for the full-bridge inverter. Taking the general P control gives rise to the steady-state error and distortion depending on the load characteristic. So, the open-loop control is the best method to avoid distortion of the output voltage. The leakage reactance and the AC capacitor connected to the inverter output terminal operate as the LC filter to cut off the harmonics due to switching operation.
The general open-loop scheme cannot generate the output voltage without distortion because it brings about overshoot and oscillation for the step change of inverter voltage. In order to solve this problem, the capacitor current is measured and its differential value is added to the inverter voltage control. This method also offers rapid rise of the output voltage. However, the magnitude of output voltage varies depending on the size of load. So, the output voltage is adjusted by calculating the effective value for one period right after the compensation is completed. This can overcome the weak point of open loop control for the output voltage.

4. Simulation

Many computer simulations with PSCAD/EMTDC software were carried out for analysing the performance of proposed DVR. The power circuit and controller were modelled as close as to the real system, using the passive and active components, and the built-in control block in PSCAD/EMTDC software. Particularly, the controller was designed using the user-defined model programmed with C code so as to implement the control action and PWM pulse generation as real as possible. It is very effective to implement the hardware controller using DSP. Table II shows the circuit parameters for a 3kVA DVR system considered in the simulation.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Rating</td>
<td>220V, 60Hz</td>
</tr>
<tr>
<td>Power Rating</td>
<td>3kVA</td>
</tr>
<tr>
<td>Source Reactance</td>
<td>0.5mH</td>
</tr>
<tr>
<td>Energy Storage Capacitor</td>
<td>1.0F</td>
</tr>
<tr>
<td>Power Transformer</td>
<td>3kVA, 220:220V, 3%</td>
</tr>
<tr>
<td>IGBT switch</td>
<td>600V, 200A</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>10kHz</td>
</tr>
</tbody>
</table>

Fig. 7a shows the source voltage, the load voltage, and the compensating current from the inverter when the 50% voltage sag occurs. The load voltage maintains a constant value because the inverter injects a nominal voltage during the sag.

Fig. 7b shows the expanded waveform focused on the sag beginning and ending point. The load voltage is restored within 2.0ms after the instant when the voltage sag occurs. This delay is due to the sag detection time and the turn-off time of thyristor switch.

Fig. 7c shows the expanded waveform at the sag beginning point.

Fig. 8a shows the source voltage, the load voltage, and the compensating current from the inverter when the voltage interruption occurs. The load voltage maintains a constant value because the inverter injects a nominal voltage during the interruption.

Fig. 8b shows the expanded waveform focused on the interruption beginning and ending point. The load voltage is restored within 2.0ms after the instant when the voltage interruption occurs. This delay is due to the interruption detection time and the turn-off time of thyristor switch. The inverter continuously supplies the load voltage for 20ms after the instant when the voltage sag restored to confirm the turn-on state of thyristor switch.

Fig. 8c shows the expanded waveform at the sag ending point.

Fig. 9a shows the source voltage, load voltage, and compensating current.
5. Prototype Experiment

A prototype of proposed DVR was built and tested to confirm the feasibility of hardware implementation, based on the simulation results. The prototype is composed of three full-bridge inverter to control each phase voltage, gate-drive circuit, super-capacitor bank, power transformer, anti-parallel thyristor switches, display circuit, and DSP controller as shown in Fig. 9. All the circuit parameters for hardware prototype are exactly same as in Table II.

One remarkable feature of proposed DVR is the fast detection and compensation, which utilizes the algorithm described in the chapter II. This fast detection algorithm can be implemented in real time operation using the high performance DSP controller. The DSP controller offers a display function, which monitors the whole system operation and indicates the number of voltage disturbances in real time.

The DSP controller was designed using TMS320vc33 DSP chip for real time operation and EPLD chip for logic implementation. The proposed DVR sets the operation frequency automatically by checking the source voltage when the system starts up. All operation is carried out automatically when the main switch is turned on.

Fig. 10a shows the source voltage, the load voltage, and the compensating current from the inverter when the 50% voltage sag occurs. The load voltage maintains a constant value as confirmed in the simulation results. Fig. 10b shows the expanded waveform focused on the sag beginning and ending point. The load voltage is restored within 2.0ms as confirmed in the simulation results. This delay is due to the sag detection time and the turn-off time of thyristor switches.
Fig. 11a shows the source voltage, the load voltage, and the compensating current from the inverter when the voltage interruption occurs. The load voltage maintains a constant value as confirmed in the simulation results. Fig. 11b shows the expanded waveform focused on the starting point of interruption. The load voltage is restored within 2.0ms as confirmed in the simulation results. This delay is due to the sag detection time and the turn-off time of thyristor switch. Through the experimental results, it is confirmed that the proposed DVR can restore the input voltage within 2.0ms from the instant when the source disturbance occurs.

![Fig. 11a: A-phase Source voltage, load voltage, compensating current](image1)

(a) A-phase Source voltage, load voltage, compensating current

![Fig. 11b: B-phase Source voltage, load voltage, compensating current](image2)

(b) B-phase Source voltage, load voltage, compensating current

![Fig. 11c: C-phase Source voltage, load voltage, compensating current](image3)

(c) C-phase Source voltage, load voltage, compensating current

![Fig. 11d: Expanded waveform of three phase load voltage at interruption beginning point](image4)

(d) Expanded waveform of three phase load voltage at interruption beginning point

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6. Conclusion

The developed detection algorithm has a hybrid structure composed of an instantaneous sag detection part and two RMS-variation detectors. The source voltage passes through the instantaneous sag detection part. If instantaneous sag is detected, the RMS variation detector-1 is selected to calculate the RMS variation. The RMS variation detector-2 is selected when the instantaneous sag occurs under the operation of the RMS variation detector-1.

The feasibility of proposed algorithm was verified through computer simulations and experiments with reference to a prototype of line-interactive three-phase DVR with 3kVA rating. The line-interactive DVR with proposed algorithm can compensate the input voltage sag and interruption within 2ms delay.

The DVR system with proposed algorithm has a maximum allowable duration of 4 seconds. It can effectively compensate the voltage interruption in sensitive loads, such as computer, automation equipment, and communication equipment. It has a simple structure to be easily implemented with commercially available components and to be highly reliable in operation.

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References


