A Comparative Study between a Conventional Two-Level and a Flying Capacitor
Four-level VSI for Use in Four-Wire Shunt APF Applications

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Abstract. Shunt Active Power Filters (SAPF) are proposed for Power Quality (PQ) improvement in perturbed power distribution networks. Conventionally, the 2-level Voltage Source Inverter (VSI) topology is used in three-phase four wire power distribution networks to mitigate current harmonics and to enhance Power Factor (PF). The Multilevel Inverter (MI) such as the Flying-Capacitor (FLC) topology is competitive with the conventionally inverters for the same targets on low voltage domain, in addition to its performance in medium voltage. In this work a comparative study of two SAPF topologies is proposed. We compare the performance for the two structures for the same modulation, same current and voltage regulation method, same control strategy using modified formulation of the p-q strategy. Firstly, it is demonstrated that the neutral current can be reduced in the conventionally 2-level structure by using a Phase Shift PWM (PSPWM) modulation instead of Sinusoidal PWM (SPWM) modulation. Secondly, peaks of source currents are reduced in the transient state by action on the Pass Band of the DC voltage regulator. Thirdly, comparison between the sizes of the inductance of the filters is made, voltage stresses on the electronic components are compared and harmonic generated by the output voltages of VSI are compared. It is demonstrated the superiority of the FLC over the two-level topology.

Keywords
Active power filter, VSI, FLC, modified p-q theory, harmonics.

Nomenclature and Formulas

<table>
<thead>
<tr>
<th>SAPF</th>
<th>Shunt Active Power Filter</th>
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<tr>
<td>APF</td>
<td>Active Power Filter</td>
</tr>
<tr>
<td>PQ</td>
<td>Power Quality</td>
</tr>
<tr>
<td>VSI</td>
<td>Voltage Source Inverter</td>
</tr>
<tr>
<td>PF</td>
<td>Power Factor</td>
</tr>
<tr>
<td>MI</td>
<td>Multilevel Inverter</td>
</tr>
<tr>
<td>FLC</td>
<td>Flying Capacitor</td>
</tr>
<tr>
<td>PSPWM</td>
<td>Phase Shift Pulse Width Modulation</td>
</tr>
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<td>SPWM</td>
<td>Sinusoidal Pulse Width Modulation</td>
</tr>
<tr>
<td>(v_{inv})</td>
<td>Output voltage of the inverter</td>
</tr>
<tr>
<td>(V_{inv})</td>
<td>Average value of the filter’s output voltage</td>
</tr>
<tr>
<td>(G_{inv})</td>
<td>Gain of the inverter</td>
</tr>
<tr>
<td>(f)</td>
<td>Frequency of the voltage source</td>
</tr>
<tr>
<td>(f_{sw})</td>
<td>Switching frequency</td>
</tr>
</tbody>
</table>

\[
THD_x = \sqrt{\sum_{n=2}^{\infty} X_n^2} \frac{X_1}{X_1}
\]

1. Introduction
Nonlinear loads such, as televisions, compact fluorescent lamps, personal computers and multimedia devices, phone chargers and battery charger for electric vehicle in addition to more other tertiary sector and industrial loads, are increasingly used in power distribution networks. All this devices absorb a non-sinusoidal current that increases the current and voltage Total Harmonic Distortion (THD) [1-4], generates a noticeable circulating current in the neutral line [5], and causes additional losses in the power transmission lines and transformers [6-9]. It is demonstrated in [10] that the voltage distortion can exceed levels set by IEEE 519 [11] due to the progressive use of nonlinear devices. The SAPF was already presented as a solution for improving PQ [12-21]. But researches are needed to improve the quality of filtering. Pulse Width Modulation PWM [22-23], is used for a VSI and MI. In this paper, we propose the Phase Shift PWM (PSPWM) modulation scheme for the VSI based-on three carriers shifted of 120° like as the modulation control for a FLC. This control insures a good control for the neutral current on the side of the source and permits a fair comparison with the FLC.

And more, in this work, a comparison on the performance of the two structure is studied on term of sizing of filter inductance, on the harmonic distortion of source currents and finally on the electronic component constraints.

This paper is organized as follows. In section 2, the SPWM and PSPWM are presented but slightly modified in order to obtain the gain of converters. Consequently, the current regulation scheme is done. In section 3, DC voltage regulation and control law for both structures are presented.
In fact, a new control strategy was developed and validated in a previous work [24-25]. In this paper, just a summary is given about this control strategy.

In section 4 a comparison is made on the performance of SAPF on PSPWM modulation scheme and classical SPWM. It is demonstrated in this section that the PSPWM is better than the SPWM for active filter operation. More, performance of the simulation based on the Pass Band of the DC voltage regulator is discussed. Also, in this section, the comparison between conventionally VSI and FLC VSI is made. The simulation results using the Psim tool are presented and discussed. The paper finally ends with some concluding remarks in section 5.

2. Modulation Techniques

A. Sinusoidal PWM

In the classical SPWM, The VSI converter is controlled using one carrier modulation strategy compared to the three reference signals illustrated in Fig. 1.

The duty cycle is given by:
\[ \alpha = \frac{t_{on}}{T_s} \]

The duty cycle is given by:
\[ \alpha = \frac{t_{on}}{T_s} = \frac{V_{ref}}{\bar{V}_p} \]  

The average value of the output voltage of the inverter is therefore:
\[ V_{inv} = \frac{E}{2}(2\alpha - 1) \]  

Replacing (2) on (3) and assuming that:
\[ \bar{V}_p = 1 \]  

The average voltage of the inverter becomes:
\[ V_{inv} = \frac{E}{2}(2V_{ref} - 1) \]

We can make a translation of \( \frac{1}{2} \) for the \( v_{ref} \) presented on Fig. 2.

\[ \frac{1}{2} + v_{ref} \]

Fig. 2. Modification of \( v_{ref} \).

The new reference is presented on Fig. 3.

According to which we may set:
\[ \alpha = \alpha_n + \alpha_{ref} \]  

With, the naturally duty cycle:
\[ \alpha_n = \frac{t_{on}}{T_s} = \frac{T_s}{T_s} = \frac{1}{2} \]  

and:
\[ \alpha_{ref} = \frac{2A_e}{T_s} = \frac{V_{ref}}{\bar{V}_p} \]  

Then:
\[ \alpha_{ref} = \alpha - \frac{1}{2} \]  

From (3) and (9), we can write:
\[ V_{inv} = \frac{E}{2}(2\alpha - 1) = \frac{E}{2}\left(2(\alpha_{ref} + \frac{1}{2} - 1)\right) = \alpha_{ref}E \]  

Finally, by using (8) and (4) on (10), we obtain:
\[ V_{inv} = V_{ref}E \]  

The gain \( G_{inv} \) of the filter is:
\[ G_{inv} = \frac{V_{inv}}{V_{ref}} = E \]  

B. Phase shift PWM

For the VSI Fig. 9, the new command consists on employing three carriers shifted by 120 degrees and compared to the three reference signals. The resulting control signals \( u_1(t), u_2(t) \) and \( u_3(t) \) are generated for each carrier. It is assumed that the switching frequency is much higher than the reference frequency.
For an FLC inverter with a three-cell structure, three carriers shifted by 120 degrees are employed and compared to the same reference signal. Three resulting control signals $u_1(t), u_2(t)$ and $u_3(t)$ are generated. By assuming the switching frequency much higher than the reference frequency, the conducting periods of the switches are practically equal on a switching cycle $T_s$, i.e.:

$$t_{1on} = t_{2on} = t_{3on} = t_{on}$$

(13)

It yields:

$$a_1 = a_2 = a_3 = \alpha$$

(14)

This assumption is essential for the operation of the FLC to ensure a natural balancing of the split DC voltages [39].

C. Electrical model for the filter

The electrical equation for the filter is:

$$v_{inv} - v_s = L_f \frac{di_f}{dt}$$

(15)

with:

$$v_{inv} = G_{inv}.v_{ref}$$

(16)

These equations are represented by the block diagram in Fig. 4.

The grid voltage $v_s$ constitutes a perturbation for the transfer function $\frac{i_f}{v_{ref}}$ which is compensated for as shown in Fig. 5.

The block diagram in Fig. 5 illustrates this regulation, with:

$$v_{ref} = \left(v_{ref} + \frac{v_s}{G_{inv}}\right).G_{inv} - v_s = v_{ref}.G_{inv}$$

(17)

The transfer function can be then written:

$$\frac{i_f}{v_{ref}} = \frac{1}{L_f.s} \Rightarrow \frac{i_f}{v_{ref}} = \frac{G_{inv}}{L_f.s}$$

(18)

Then:

$$\frac{i_f}{v_{ref}} = \frac{G_{inv}}{L_f.s} = \frac{E}{L_f.s}$$

(19)

3. DC Voltage Regulation and Control Strategy

A. DC voltage regulation

For the harmonics filtering and PF compensation, there is no need for energy storage on the capacitor. Otherwise, the capacitor would need an active power to replace energy used to compensate the losses on the filter. This leads to stabilize the DC bus voltage. The energy stored on the capacitor is:

$$w = \frac{1}{2}.C.V^2$$

(20)

That gives for the instant power:

$$p = \frac{dv}{dt} = \frac{1}{2}.C.\frac{dv^2}{dt}$$

(21)

By setting:

$$X = V^2$$

it yields:

$$p = \frac{1}{2}.C.\frac{dX}{dt}$$

(22)

and, in the Laplace domain:

$$P(s) = \frac{1}{2}.C.s.X(s)$$

(24)

The transfer function is:

$$\frac{x(s)}{P(s)} = \frac{2}{c.s}$$

(25)

On the other hand, the total power absorbed at the source for the two capacitors is:

$$P = \frac{3\tilde{V}i}{2} = \frac{3\tilde{V}i_f}{2}$$

(26)

For one capacitor:

$$P = \frac{3\tilde{V}i_f}{4}$$

(27)

The block diagram in Fig. 6 illustrates this regulation, with:

$$k_p = \frac{2.C.\omega_{pu}}{3.P}$$

(28)

and:

$$T_i = \frac{\sqrt{36}}{\omega_{pu}}$$

(29)

B. Control strategy

A new expression of the reference currents is developed in the method described in [24-25]. This method is based on
the separation of the zero sequence current from the zero sequence power in the case of balanced voltages and unbalance and distorted currents, which has permitted to control an equal repartition of the zero-sequence current component within the three phases of the supply distribution network yielding, thereby, the elimination of the neutral current. A brief description of this method follows.

Powers in the $ab\beta$ frame are given by the following equation:

$$\begin{bmatrix} P \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha \\ -v_\beta \\ v_\alpha \end{bmatrix} \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \cdot \begin{bmatrix} \bar{p} + p_c \\ \bar{q} \\ \bar{q} \end{bmatrix}$$  \hspace{1cm} (30)

Current references in $ab\beta$ frame are consequently given by:

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \frac{1}{2 \sqrt{2}} \begin{bmatrix} 0 \\ 1 \\ -1 \end{bmatrix} \cdot \begin{bmatrix} v_\alpha \\ -v_\beta \\ v_\alpha \end{bmatrix} \\ \frac{1}{2 \sqrt{2}} \begin{bmatrix} 0 \\ 1 \\ -1 \end{bmatrix} \cdot \begin{bmatrix} \bar{p} + p_c \\ \bar{q} \\ \bar{q} \end{bmatrix}$$  \hspace{1cm} (31)

The current references in $abc$ frame are computed as:

$$\begin{bmatrix} i_a^* \\ i_b^* \\ i_c^* \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 0 \\ 1 \sqrt{3} \\ 2 \end{bmatrix} \cdot \begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} + \frac{1}{\sqrt{3}} \begin{bmatrix} 1 \sqrt{3} \\ 2 \end{bmatrix} \cdot \begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix} + \frac{1}{\sqrt{3}} \begin{bmatrix} 0 \\ 2 \sqrt{3} \end{bmatrix} \cdot \begin{bmatrix} \bar{q} \end{bmatrix}$$  \hspace{1cm} (32)

The block diagram in Fig.7 illustrates this method, where $P_c$ represents the losses power. Fig. 8 represents the scheme of the regulation of current.

![Fig. 7. Block diagram for reference currents extraction.](image)

**Fig. 7. Block diagram for reference currents extraction.**

![Fig. 8. Block diagram for current regulation and modulation.](image)

**Fig. 8. Block diagram for current regulation and modulation.**

### 4. Simulation Results and Discussions

All experiments are made with the following numerical values:

- Source: $V = 310V$, $f = 50Hz$
- 2-level VSI inverter : $C = 1 \text{ mF}$, $L = 12 \text{ mH}$
- FLC inverter: $C = 1 \text{ mF}$, $L = 2 \text{ mH}$
- Modulation frequency: $f_{pbv}=10 \text{ kHz}$
- Regulators: $f_{pbv}=3\text{kHz}$, $f_{pbv}=300 \text{ Hz}$
- Resistive loads: $R_1=6\text{ mH}$, $R_2=8\text{ mH}$, $R_3=10\text{ mH}$
- Common load: $L_1=6 \text{ mH}$, $L_2=0.5\text{ mH}$, $L_3=20 \text{ mH}$, $C=1500\text{ mF}$

### A. Effect of the voltage loop crossing frequency

A good filtering is the result of a compromise between the method of reference currents extraction, modulation and regulators for currents and voltages. In what follows, we consider that the current absorbed by the capacitors, for the compensation of losses, is passed through the diodes of the inverter and its frequency is 6f. Then, the crossing frequency of the DC voltage regulator is chosen for $f_{pbv}=300\text{Hz}$. Fig. 9 illustrates the three levels FLC based on APF.
the peaks on source currents are greater. In the following, 
\( f_{\text{sw}} = 300 \text{ Hz} \) is adopted for simulations.

In Fig. 10.e, the load currents are show and, in Table 2, their THD values are given.

In Fig. 11, the load currents are shown and, in Table 2, their THD values are given.

**Fig. 10.** Comparison between phase-neutral voltages for the two modulation techniques.

**Fig. 11.** VSI 2-level scheme on APF application.

**C. Comparison between the VSI and FLC**

Once we have the same modulation, the same control strategy and the same voltage regulator, the comparison on the structures is fairly carried and gives a better appreciation. The main difference is on the size of the filter inductance. Fig. 14 shows that the performance of the two structures cannot be approached except for a value of filter inductance for the 2-level equal to 6 times that of the FLC. Figs. 14.a and 14.b show the source currents for, respectively, 2-level and FLC and in Table 2, the THD values prove the excellent advantage of the FLC. In Fig. 14.d, neutral current on the source side for an APF based-on FLC is more reduced than that the neutral current for 2-levels VSI on Fig. 14.c. Harmonic contents within the phase to neutral voltage Figs. 14.e and 14.f are of interest in the FLC and more, the first harmonic appears at 3\( f_{\text{sw}} \) for the FLC in Fig. 14.f and at \( f_{\text{sw}} \) for the 2-level topology. In Fig. 14.g and Fig. 14.h, the spectrum of the IGBT voltage shows that amplitudes of harmonics in the FLC (200 V for DC component) are lower than that the 2-level (600V for DC component). This result means that the harmonic stress on the IGBT of FLC topology is much reduced. It is a main advantage for a multilevel inverter.

5. **Conclusions**

In this work, a comparison is made between two topologies of VSI for SAPF application. It is validate by simulation for the FLC use that the neutral current on the side of the source is reduced more than that the 2-levels. Harmonic distortion of the source currents is also more reduced. These results are obtained with initially improvement for the functioning of the 2-level by using the PSPWM instead the SPWM modulation. The size of the filter inductor for a FLC is much smaller than that the 2-levels. Small amplitude of harmonic on the output voltage of the filter and the frequency of the first harmonic (3\( f_{\text{sw}} \)) for the FLC leads to sizing a small output filter. The maximum of the voltage across IGBTs is reduced three times for the FLC versus the 2-levels. The FLC topology is shown to be better than the 2-level conventional inverter for APF applications.

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References


Table 1: Harmonic components for the phase to neutral voltage.

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<tr>
<th>harmonics</th>
<th>SPWM</th>
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<tr>
<td>50Hz</td>
<td>338</td>
<td>340</td>
</tr>
<tr>
<td>150 Hz</td>
<td>91</td>
<td>90</td>
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<td>250 Hz</td>
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<td>35</td>
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<td>350 Hz</td>
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<td>31</td>
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<tr>
<td>450 Hz</td>
<td>36</td>
<td>14</td>
</tr>
<tr>
<td>550 Hz</td>
<td>60</td>
<td>50</td>
</tr>
<tr>
<td>10 kHz</td>
<td>558</td>
<td>551</td>
</tr>
<tr>
<td>19950</td>
<td>74</td>
<td>73</td>
</tr>
<tr>
<td>20050</td>
<td>126</td>
<td>118</td>
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</table>

Table 2: Comparative values of THD for the source currents.

<table>
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<tr>
<th>Load currents</th>
<th>THDsi</th>
<th>Source currents</th>
<th>SFWM 2-level</th>
<th>PSPWM 2-level</th>
<th>PSPWM FLC</th>
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<tr>
<td>iLa</td>
<td>17%</td>
<td>iSa</td>
<td>2.3%</td>
<td>2.2%</td>
<td>1.42%</td>
</tr>
<tr>
<td>iLb</td>
<td>18%</td>
<td>iSb</td>
<td>2.32%</td>
<td>2.24%</td>
<td>1.49%</td>
</tr>
<tr>
<td>iLc</td>
<td>19%</td>
<td>iSc</td>
<td>2.36%</td>
<td>2.29%</td>
<td>1.38%</td>
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</table>

Fig. 1.4. Comparison between a VSI 2-levels and FLC.


